Ultra-small Dual 40 mΩ 1.0 A Integrated Power Switch with Discharge

General Description

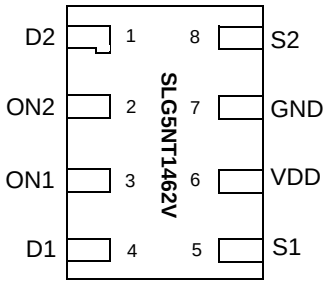
The SLG5NT1462V is designed for power switching applications. The part comes with two 40 mΩ 1.0 A rated MOSFETs, each controlled by an ON control pin. Each MOSFET's ramp rate is adjustable depending on the input current level of the ON pin.

The product is packaged in an ultra-small 1.6 x 1.0 mm package.

Features

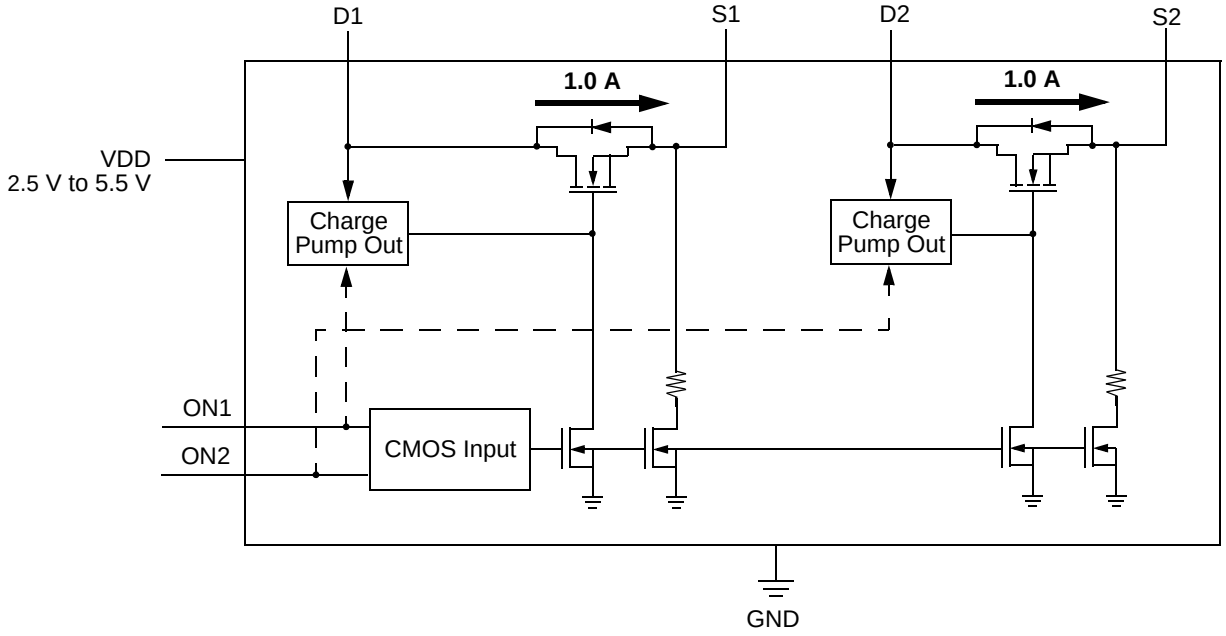
- Two 40 mΩ 1.0 A MOSFETs
- Two integrated VGS Charge Pumps
- User selectable ramp rate with external resistor
- Protected by thermal shutdown
- Integrated Discharge Resistor
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 8L, 1.0 x 1.6 mm

Pin Configuration



8-pin STDFN
(Top View)

Block Diagram



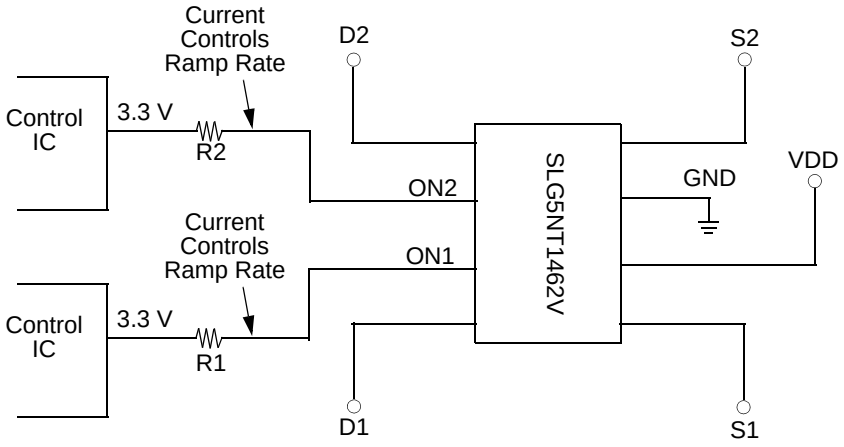
Pin Description

Pin #	Pin Name	Type	Pin Description
1	D2	MOSFET	Drain of Power MOSFET1
2	ON2	Input	Turns on MOSFET1. Configurable slew rate control depending on input current.
3	ON1	Input	Turns on MOSFET2. Configurable slew rate control depending on input current.
4	D1	MOSFET	Drain of Power MOSFET2
5	S1	MOSFET	Source of Power MOSFET2
6	VDD	PWR	Power Supply
7	GND	GND	Ground
8	S2	MOSFET	Source of Power MOSFET1

Ordering Information

Part Number	Type	Production Flow
SLG5NT1462V	STDFN 8L	Industrial, -40 °C to 85 °C
SLG5NT1462VTR	STDFN 8L (Tape and Reel)	Industrial, -40 °C to 85 °C

Application Diagram



Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply		--	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
θ_{JA}	Thermal Resistance,	1 x 1.6mm STDFN; Determined using 1 in^2, 1 oz. copper pads under each Dx and Sx terminal and FR4 pcb material	--	72	--	°C/W
W_{DIS}	Package Power Dissipation		--	--	0.4	W
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply	Pin 6	2.5	--	5.5	V
V_{D1}	Drain Voltage of MOS1	Pin 4	0.85	--	V_{DD}	V
V_{D2}	Drain Voltage of MOS2	Pin 1	0.85	--	V_{DD}	V
I_{DD}	Power Supply Current (PIN 6)	when OFF	--	0.1	1	µA
		when ON, No load	--	35	50	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A 25°C MOSFET[1:2] @ 100 mA	--	40	50	mΩ
		T_A 70°C MOSFET[1:2] @ 100 mA	--	50	55	mΩ
		T_A 85°C MOSFET[1:2] @ 100 mA	--	55	65	mΩ
IDS	Operating Current	V_D = 2.5 V to 5.5 V	--	--	1.0	A
T_{Delay_ON}	ON pin Delay Time	50% ON to Ramp Begin Input Current (PIN2, PIN3) = 20 µA, V_{DD} = V_D = 5 V, Source_Cap = 10 µF, R_L = 20 Ω	--	2.4	4.0	ms
T_{Total_ON}	Total Turn On Time	50% ON to 90% V_S	Configurable [1]			ms
		Example: Input Current (PIN2, PIN3) = 20 µA, V_{DD} = V_D = 5 V, Source_Cap = 10 µF, R_L = 20 Ω	--	11.7	--	ms
$T_{SLEWRATE}$	Slew Rate	10% V_S to 90% V_S	Configurable [1]			V/ms
		Example: Input Current (PIN2, PIN3) = 20 µA, V_{DD} = V_D = 5 V, Source_Cap = 10 µF, R_L = 20 Ω	--	0.56	--	V/ms
R_{DIS}	Discharge Resistance		100	150	300	Ω
ON_V_{REF}	ON Pin Reference Voltage [2]		0.99	1.05	1.10	V
$ON\_V_{IH\_INI}$	Initial Turn On Voltage	Internal Charge Pump ON	1.2	--	V_{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin	Internal Charge Pump OFF	-0.3	0	0.3	V
ON_R	Input Impedance on ON pin		100	--	--	MΩ
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	125	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	100	--	°C
$THERM_{TIME}$	Thermal shutoff time		--	--	1	ms

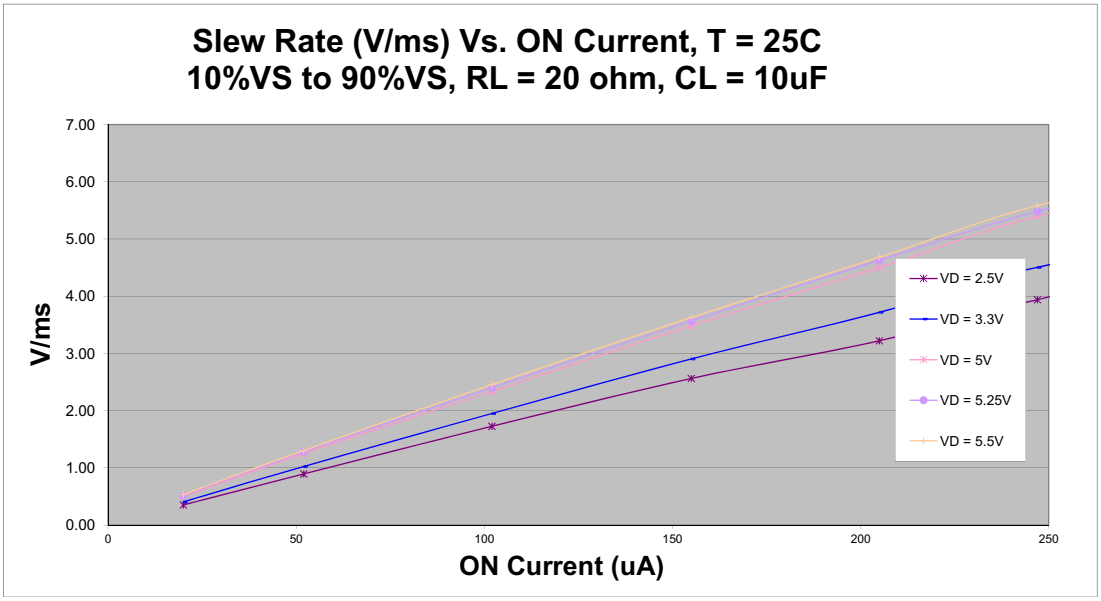
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

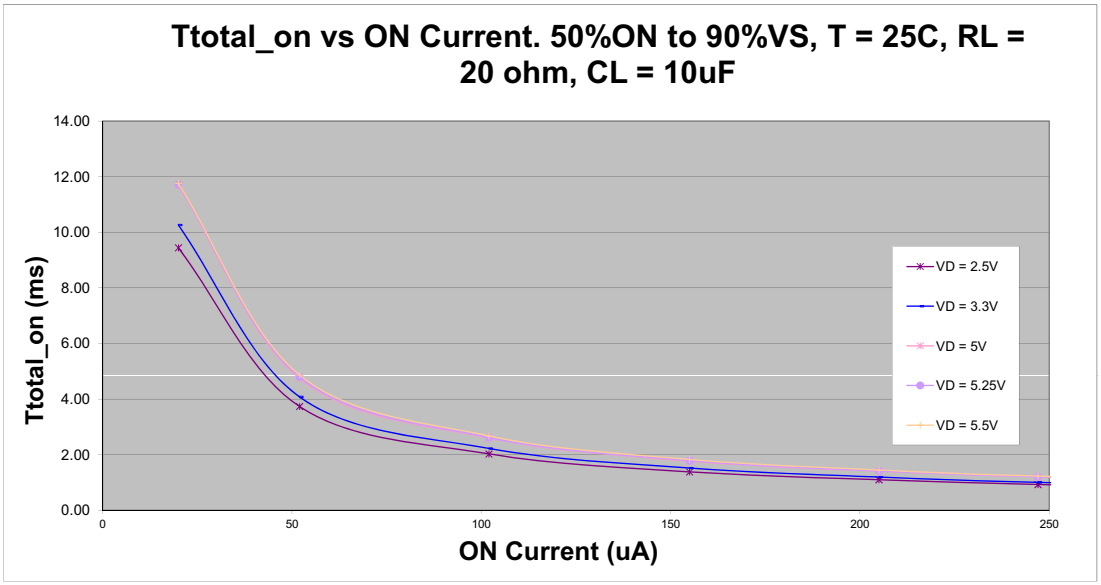
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T_{OFF_Delay}	OFF Delay Time	50% ON to V_S Fall, V_D = 5 V, R_L = 20 Ω, no C_L	--	55	70	µs
T_{FALL}	V_S Fall Time	90% V_S to 10% V_S, V_D = 5 V, R_L = 20 Ω, no C_L	--	32	--	µs

Notes:
1. Refer to table for configuration details.
2. Voltage before ON pin resistor needs to be higher than 1.2 V to generate required I_{ON}

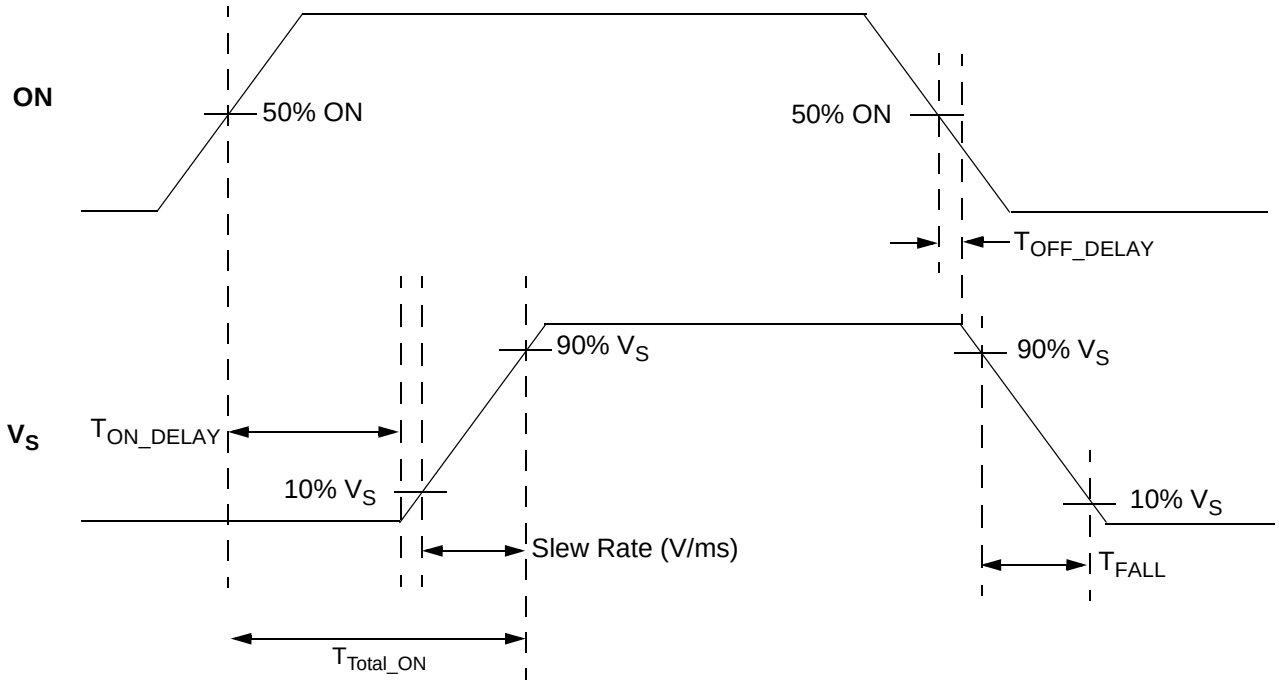
Slew Rate vs. ON Current



T_{Total_ON} vs. On Current



T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



Adjustable Ramp Rate vs. ON Pin Current (5.5 V, 25 °C)

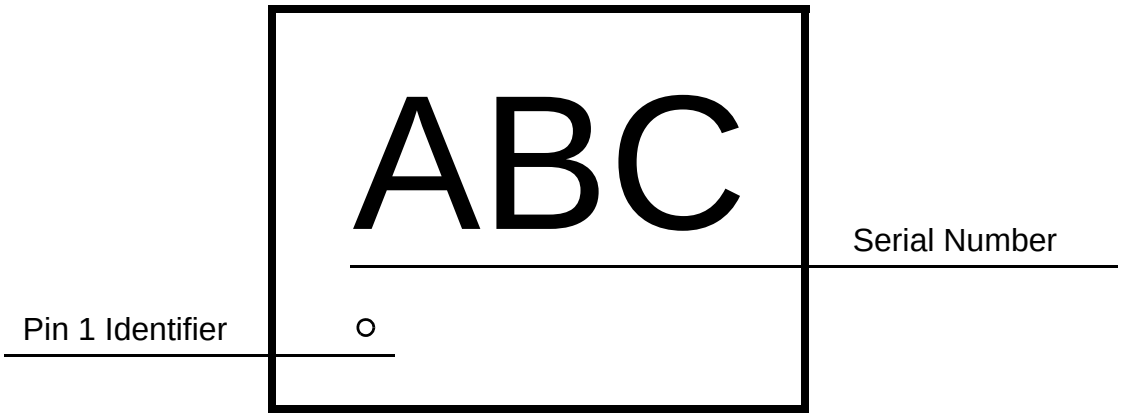
I_ON	T_{SLEW} (typ)
20 µA	0.56 V/ms
50 µA	1.34 V/ms
100 µA	2.53 V/ms
150 µA	3.71 V/ms
200 µA	4.68 V/ms
250 µA	5.63 V/ms

Adjustable Slew Rate (ON2 Pin 2 and ON1 Pin3)

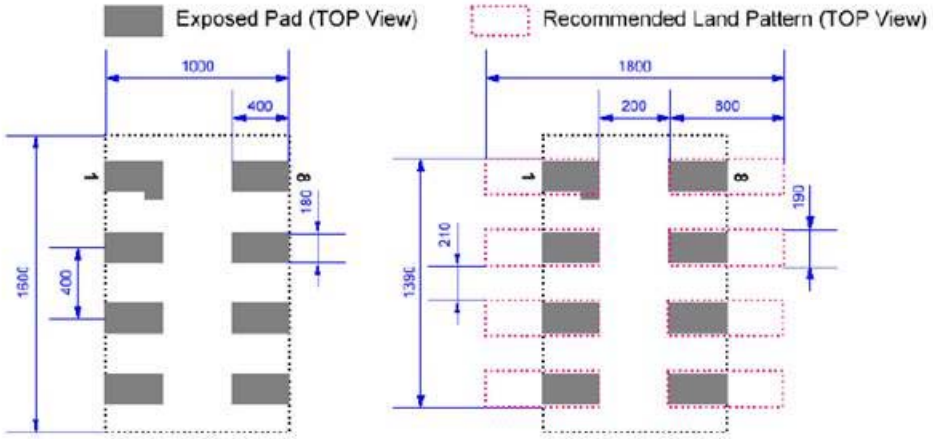
SLG5NT1462V has a built in configurable slew control feature. The configurable slew control uses current detection method on ON1/ON2. When ON voltage rise above ON_VIH_INI (1.2 V typical), the slew control circuit will measure the current flowing into ON1/ON2. Based on the current flowing into ON1/ON2, different slew rates will be selected by the internal control circuit. See I_ON vs. Tslew table. The slew rate is configurable by selecting a different R1/R2 resistor value as shown on application diagram. Calculating the R1/R2 value depends on both the desired slew rate, and the VOH level of the device driving the ON1/ON2 pin.

ON_Current = (GPIO_VOH – ON_VREF (1.05 V typical)) / R

Package Top Marking System Definition

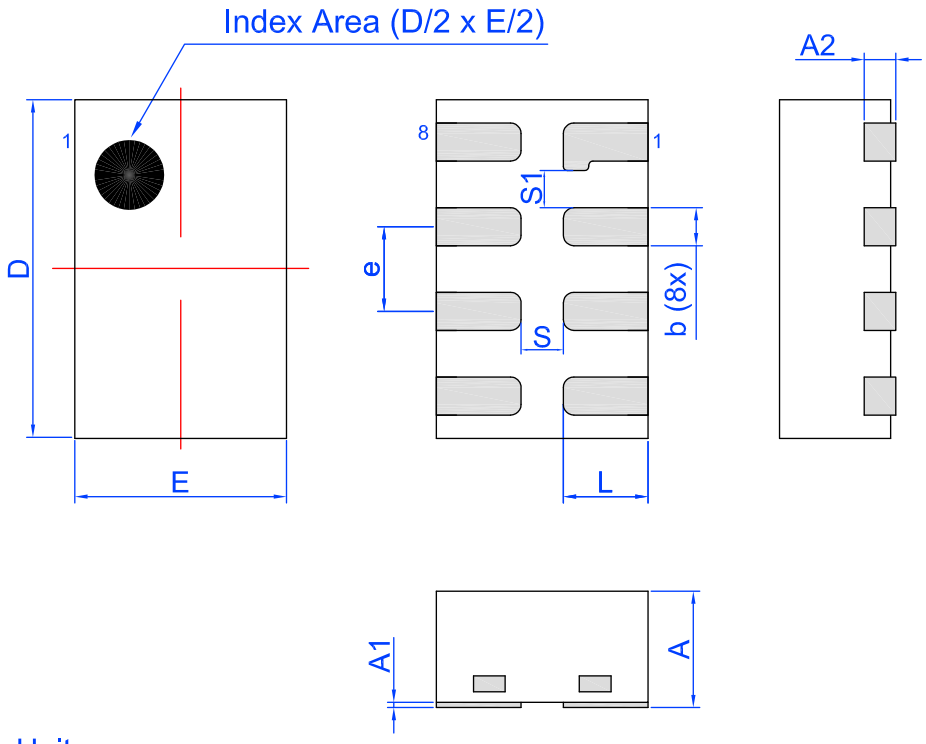


SLG5NT1462V Layout Suggestion



Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm



Unit: mm

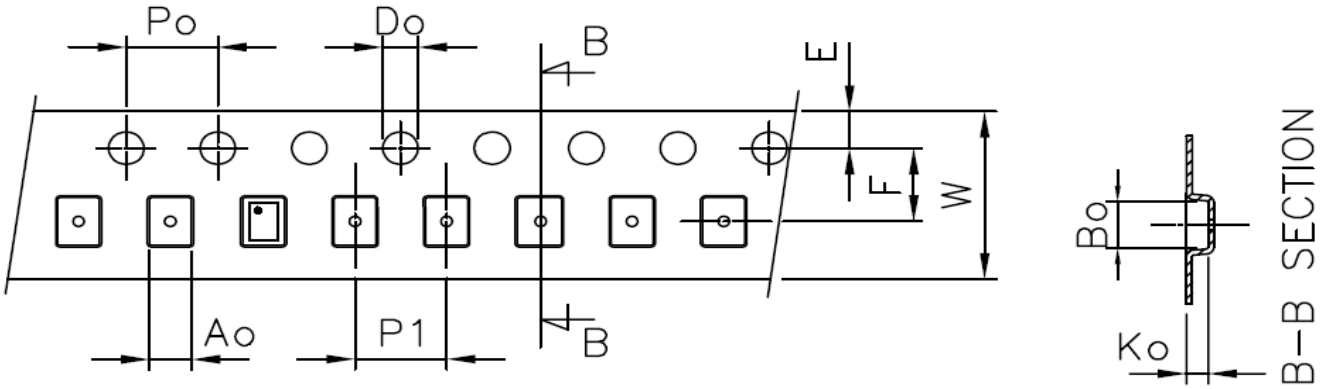
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	S	0.2 REF		
e	0.40 BSC			S1	0.175 REF		

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
12/4/2015	1.03	Updated Block Diagram
11/20/2015	1.02	Added ESD_{CDM}, MSL, and θ_{JA} specs