Freescale Semiconductor
Product Brief

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MPC5607B Microcontroller Product Brief

This document provides an overview and describes the features of the MPC5607B series of microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. For electrical specifications, pin assignments, and package diagrams, refer to the device data sheet.

The MPC5607B belongs to an expanding family of 32-bit automotive microcontrollers designed to address body electronics applications within the vehicle. The MPC5607B MCU is built on the Power Architecture® and extends the MPC560xB device family by offering additional flash memory and other features.

The advanced and cost-efficient e200z0h host processor core of this automotive controller family complies with the Power Architecture embedded category, which is 100 percent user-mode compatible with the original PowerPC user instruction set architecture (UISA). It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development

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infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with user's implementations (refer to Section 4, "Developer environment for more information).

The MPC5607B platform has a single level of memory hierarchy and can support a wide range of on-chip static random access memory (SRAM) and internal flash memory. Refer to Table 2 for specific memory and feature sets of the proposed roadmap product members.

1 Block diagram

Figure 1 shows a top-level block diagram of the MPC5607B family. Table 1 provides further details on the block functions.

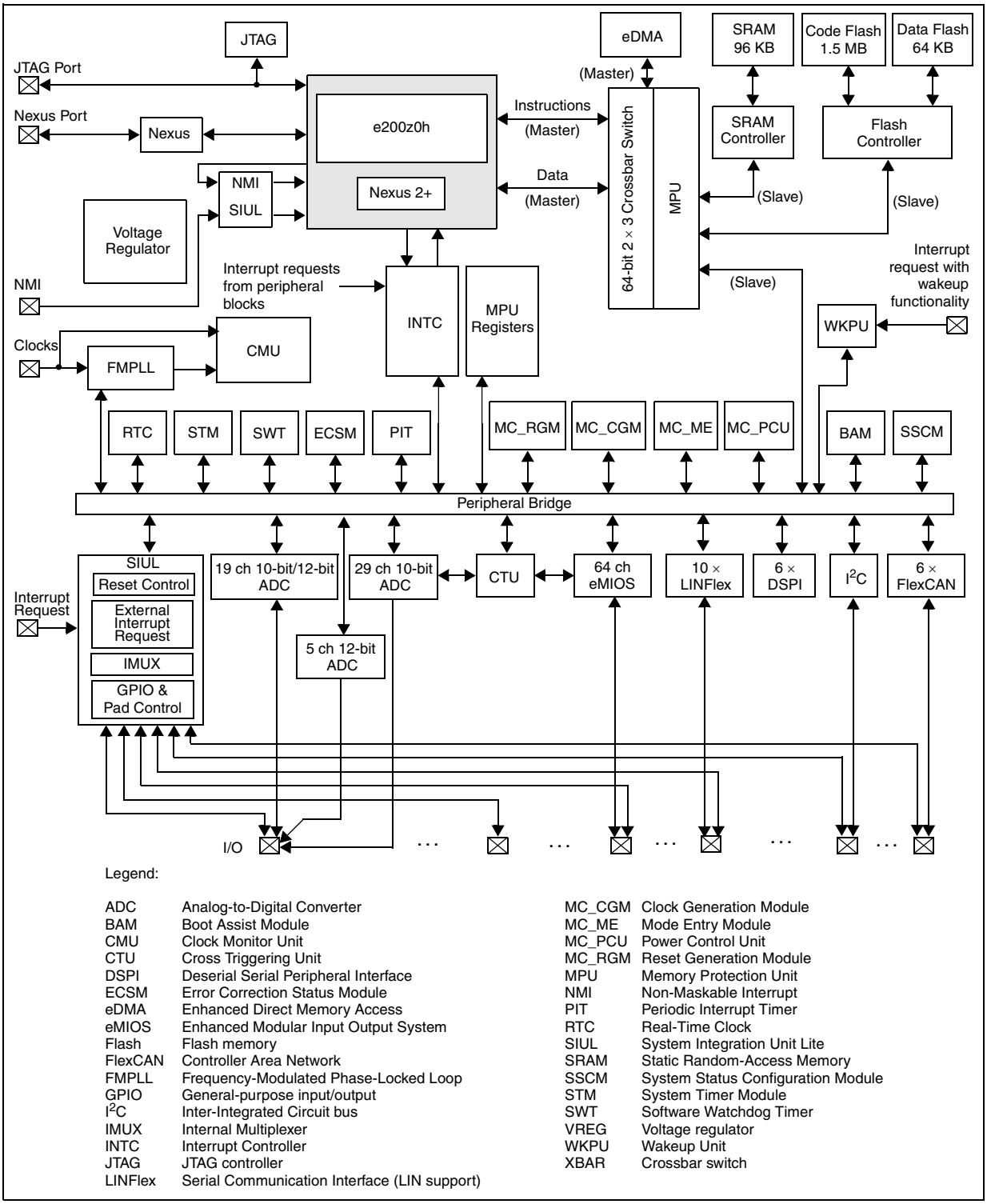


Figure 1. MPC5607B block diagram

Table 1. MPC5607B series block summary

Block	Function
Analog-to-digital converter (ADC)	Converts analog voltages to digital values
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Crossbar switch (XBAR)	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Enhanced direct memory access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via "*n*" programmable channels
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Error correction status module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
Frequency-modulated phase-locked loop (FMPLL)	Generates high-speed system clocks and supports programmable frequency modulation
Inter-integrated circuit (I^2C) bus	Two-wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller (JTAGC)	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINFlex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and modetransition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Non-maskable interrupt (NMI)	Handles external events that must produce an immediate response, such as power down detection

Table 1. MPC5607B series block summary (continued)

Block	Function
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System integration unit lite (SIUL)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
System status and configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR (Automotive Open System Architecture) and operating system tasks
Software watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 27 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.

2 Application examples

The MPC5607B is designed to address central body, vehicle body controllers, smart junction box and front module applications, and to support sensorless motor control with ripple counting within the vehicle. As shown in the following example, the MCU is central to the application and provides the flexibility to add or remove peripheral components in a modular design.

2.1 Body controller application example

Body controller modules primarily control the following:

- Comfort features: doors, seats, interior lighting
- Security/access features: passive entry, immobilizer, TPMS (tire pressure monitoring system)
- Lighting: headlights, brake lights, turn lights
- Centralized diagnostic and network management
- Vehicle communications network routing: CAN

Figure 2 shows the MPC5607B used in a typical body controller application.

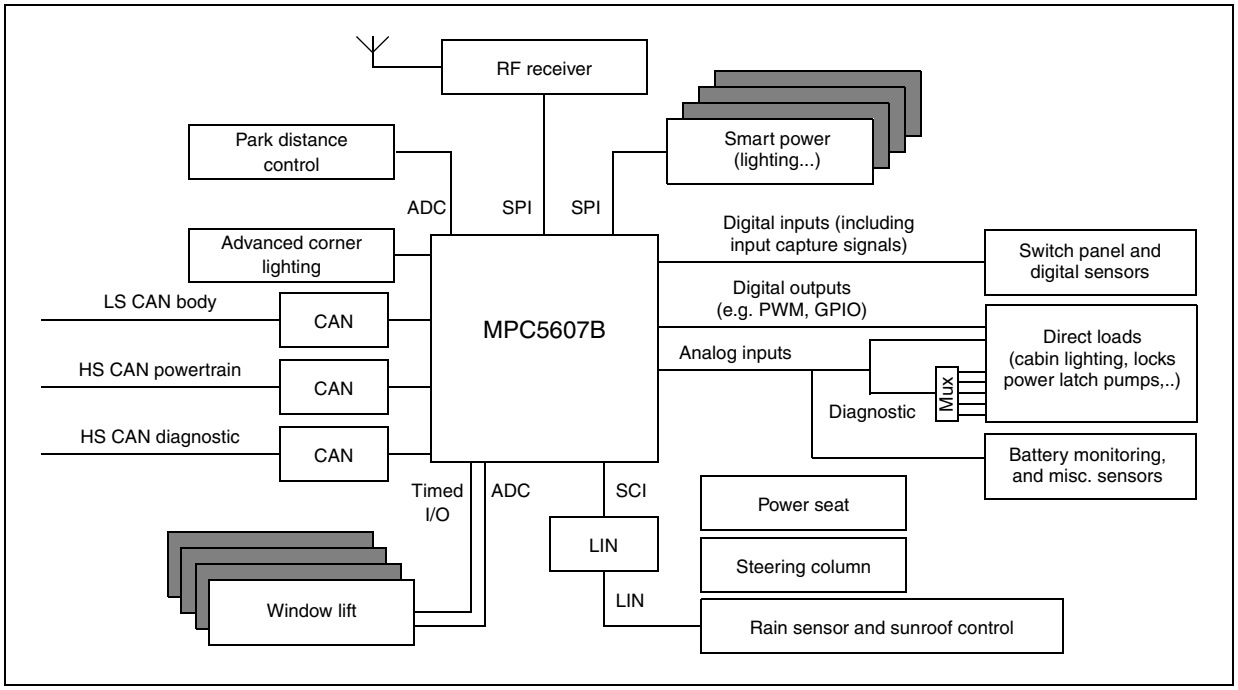


Figure 2. Body controller application example

3 Device family overview

This section provides a comparison of the different MPC5607B family members, presents the critical performance parameters, and lists both the chip-level and module features as well as the available packages.

3.1 MPC5607B family comparison

Table 2 provides a comparison summary of the different MPC5607B family members and their proposed features. This information is intended to provide an understanding of the range of functionality offered by this family.

Table 2. MPC5607B family comparison[1]

Feature	MPC5605B	MPC5606B	MPC5607B
CPU	e200z0h		
Execution speed[2]	Up to 64 MHz		
Code flash memory	768 KB	1 MB	1.5 MB
Data flash memory	64 (4 × 16) KB		
SRAM	64 KB	80 KB	96 KB
MPU	8-entry		
eDMA	16 ch		
10-bit ADC	Yes		

Table 2. MPC5607B family comparison[1] (continued)

Feature	MPC5605B			MPC5606B		MPC5607B
dedicated[3]	7 ch	15 ch	29 ch	15 ch	29 ch	
shared with 12-bit ADC	19 ch					
12-bit ADC	Yes					
dedicated[4]	5 ch					
shared with 10-bit ADC	19 ch					
Total timer I/O[5] eMIOS	37 ch, 16-bit	64 ch, 16-bit				
Counter / OPWM / ICOC[6]	10 ch					
O(I)PWM / OPWFMB / OPWMCB / ICOC[7]	7 ch					
O(I)PWM / ICOC[8]	7 ch	14 ch				
OPWM / ICOC[9]	13 ch	33 ch				
SCI (LINFlex)	4	8	10	8	10	
SPI (DSPI)	3	5	6	5	6	
CAN (FlexCAN)	6					
I^2C	1					
32 KHz oscillator	Yes					
GPIO[10]	77	121	149	121	149	
Debug	JTAG					N2+
Package	100 LQFP	144 LQFP	176 LQFP	144 LQFP	176 LQFP	176 LQFP	208 MAP BGA[11]

NOTES:
1. Feature set dependent on selected peripheral multiplexing; table shows example
2. Based on 125 °C ambient operating temperature
3. Not shared with 12-bit ADC, but possibly shared with other alternate functions
4. Not shared with 10-bit ADC, but possibly shared with other alternate functions
5. See the eMIOS section of the chip reference manual for information on the channel configuration and functions.
6. Each channel supports a range of modes including Modulus counters, PWM generation, Input Capture, Output Compare.
7. Each channel supports a range of modes including PWM generation with dead time, Input Capture, Output Compare.
8. Each channel supports a range of modes including PWM generation, Input Capture, Output Compare, Period and Pulse width measurement.
9. Each channel supports a range of modes including PWM generation, Input Capture, and Output Compare.
10. Maximum I/O count based on multiplexing with peripherals
11. 208 MAPBGA available only as development package for Nexus2+

3.2 Critical performance parameters

The critical performance parameters of the MPC5607B feature the following:

- Fully static design operation up to a maximum of 64 MHz, based on 125 °C ambient temperature

- Low-power design
  - Designed for dynamic power management of core and peripherals
  - Software-controlled clock gating of peripherals
  - Multiple power domains to minimize leakage in low-power modes
- Internal voltage regulator (VREG) enables control with a single input voltage for device operation below 100 mA with optional external ballast resistor for supporting maximum performance
  - 3.3 or 5 V ± 10% input supply voltage
- ADC analog supply 3.3 or 5 V ± 10%
- Configurable pins
  - Selectable pull-up, pull-down, or no pull on all GPIO pins
  - Selectable open-drain pin
- Frequency-modulated phase-locked loop
- –40 to 125 °C ambient operating temperature range[1]

Table 3. Operating mode summary[1]

Operating modes		SOC features				Clock sources				Periodic wakeup	Wakeup input	VREG mode	Wakeup time[2]						
		Core	Peripherals	Flash	SRAM	PLL	16 MHz FIRC	XOSC	128 kHz SIRC				VREG startup	IRC wakeup	Flash recovery	OSC stabilization	PLL lock	S/W reconfiguration	Mode switch over
RUN		On	OP	OP	On	OP	On	OP	On	—	—	FP	—	—	—	—	—	—	—
HALT		CG	OP	OP	On	OP	On	OP	On	OP	OP	FP	—	—	—	—	—	—	TBD[3]
STOP		CG	OP	APD	On	CG	OP	OP	On	OP	OP	LP	25 µs	8 µs	>125 µs	8 ms	200 µs	—	33 µs
STANDBY	1	Off	Off	Off	32 KB[4]	Off	OP	Off	OP	OP	OP	LP	25 µs	8 µs	>125 µs	8 ms	200 µs	Var	33 µs
	2	Off	Off	Off	8 KB[5]	Off	OP	Off	OP	OP	OP	LP	25 µs	8 µs	>125 µs	8 ms	200 µs	Var	33 µs
POR		—	—	—	—	—	—	—	—	—	—	—	250 µs	8 µs	>125 µs	8 ms	200 µs	—	BAM

1. Assuming that the absolute maximum of 150 °C junction temperature is respected

NOTES:
1. Table key:
   APD: Analog power-down
   BAM: Boot Assist Module Software and Hardware used for device startup and configuration
   CG: Clock Gated, Powered but clock stopped
   FP: VREG Full Performance mode
   LP: VREG Low Power mode, reduced output capability of VREG but lower power consumption
   Off: Powered off and clock gated
   On: Powered and clocked
   OP: Optionally configurable to be enabled or disabled (clock gated)
   POR: Power-on reset
   Var: Variable duration, based on the required reconfiguration and execution clock speed configuration
2. A high level summary of some key durations that need to be considered when recovering from low-power modes. This does not account for all durations at wakeup. Other delays will be necessary to consider including, but not limited to the external supply startup time.
   IRC wakeup time must not be added to the overall wakeup time as it starts in parallel with the VREG.
   All other wakeup times must be added to determine the total startup time. For example, out of STANDBY, if Flash is needed, the total wakeup time will be 120 µs.
3. TBD: To be defined
4. 32 KB of RAM content retained but not accessible in STANDBY mode
5. 8 KB of RAM content retained but not accessible in STANDBY mode

3.3 Low-power operation

MPC5607B devices provide two dynamic power modes—RUN and HALT—and two static low-power modes—STANDBY and STOP.

Both low-power modes use clock gating to halt the clock for all or part of the device. Additionally, the STANDBY mode uses power gating to automatically turn off the power supply to parts of the device to minimize leakage.

RUN modes are the main operating modes where the entire device can be powered and clocked. Four dynamic RUN modes are supported: RUN0 – RUN3. The ability to configure and select different RUN modes enables different clocks and power configurations to be supported with respect to each other and to allow switching between different operating conditions. The necessary peripherals, clock sources, clock speed and systems clock prescalers can be independently configured for each of the four RUN modes of the device.

HALT mode is a reduced activity, low power mode intended for moderate periods of lower processing activity. In this mode the core system clocks are stopped but user-selected peripheral tasks can continue to run. It can be configured to provide more efficient power management features (switch-off PLL, Flash memory, main regulator, etc.) at the cost of longer wake up latency. The system returns to RUN mode as soon as an event or interrupt is pending.

STOP mode maintains power to the entire device allowing the retention of all on-chip registers and memory, and providing a faster recovery low power mode than the lowest STANDBY mode. There is no need to reconfigure the device before executing code. The clocks to the core and peripherals are halted and can be optionally stopped to the oscillator or PLL at the expense of a slower start-up time.

STOP is entered from RUN mode only. Wakeup from STOP mode is triggered by an external event or by the internal periodic wakeup, if enabled.

STANDBY mode halts the clock to the entire device and turns off the power to the majority of the chip to offer the lowest power consumption mode.

The device can be woken up from STANDBY mode by any of up to 27 external wakeup pins, a reset, or from a periodic wakeup using a low-power oscillator. If required by the user, it is possible to enable the internal 16 MHz or 128 kHz RC oscillator or external 32 kHz oscillator.

In STANDBY mode, the contents of the cores, on-chip peripheral registers and potentially some of the volatile memory are not held:

- STANBDY2 mode retains 32 KB of the SRAM
- STANDBY1 mode retains 8 KB of the SRAM

A fast wakeup using the on-chip 16 MHz internal RC oscillator allows rapid execution from SRAM on exit from low-power modes. This oscillator supports low speed code execution and clocking of peripherals through selection as the system clock, and it can be used as the PLL input clock source to provide fast startup without the external oscillator delay.

In low-power modes, the internal 16 MHz RC oscillator also supports the operation of ADCs.

Additionally, a fast startup internal voltage regulator provides a rapid exit from low-power modes.

3.4 Chip-level features

On-chip modules available within the family include the following features:

- Single issue, 32-bit CPU core complex (e200z0h)
  - Compliant with the Power Architecture embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 1.5 MB on-chip flash memory supported with the Flash controller
- Up to 96 KB on-chip SRAM
- Memory protection unit (MPU) with 8 region descriptors and 32-byte region granularity on certain family members (see Table 2 for details)
- Interrupt controller (INTC) capable of handling 231 selectable-priority interrupt sources
- Frequency-modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash memory, or SRAM from multiple bus masters
- 16-channel eDMA controller with multiple transfer request sources using DMAMUX
- Boot assist module (BAM) supports internal Flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS)
- 2 analog-to-digital converters (ADCs)

- Cross Trigger Unit (CTU) to enable synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
- Up to 6 serial peripheral interface (DSPI) modules
- Up to 10 serial communication interface (LINFlex) modules
- Up to 6 enhanced full CAN (FlexCAN) modules with configurable buffers
- 1 inter-integrated circuit (I^2C) interface module
- Up to 149 configurable general purpose pins supporting input and output operations (package dependent)
- Real-Time Counter (RTC)
  - Clock source from internal 128 kHz or 16 MHz oscillator supporting autonomous wakeup with 1 ms resolution with maximum timeout of 2 seconds
  - Optional support for RTC with clock source from external 32 kHz crystal oscillator, supporting wakeup with 1 sec resolution and maximum timeout of 1 hour
- 8 periodic interrupt timers (PITs) with 32-bit counter resolution
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus
- Device/board boundary scan testing supported per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

3.5 Module features

The following sections provide more details of the modules implemented on the chip.

3.5.1 e200z0h core processor

The e200z0h core includes the following features:

- High performance, low cost e200z0h core processor for managing peripherals and interrupts
- Single issue 4-stage pipelined in-order execution, 32-bit Power Architecture CPU
- Variable length encoding (VLE), allowing mixed 16-bit and 32-bit instructions
  - Results in efficient code size footprint
  - Minimizes impact on performance
- Branch processing acceleration using lookahead instruction buffer
- Load/store unit
  - 1-cycle load latency
  - Misaligned access support
  - No load-to-use pipeline bubbles
- 32-bit general purpose registers (GPRs)
- Harvard architecture with separate instruction and load/store bus
- Hardware vectored interrupt support
- Reservation instructions for implementing read-modify-write constructs

- Multi-cycle divide word (divw) and load multiple word (lmw) store multiple word (smw) multiple class instructions, can be interrupted to prevent increases in interrupt latency
- Extensive system development support through Nexus debug port

3.5.2 Crossbar switch (XBAR)

The following summarizes the chip's implementation of the crossbar switch:

- 3 master ports:
  - CPU instruction bus
  - CPU load/store bus
  - eDMA
- Multiple bus slaves to enable access to flash memory, SRAM and peripherals
- Crossbar supports up to 2 consecutive transfers at any one time
- 32-bit internal address bus, 32-bit internal data bus
- Fixed priority arbitration based on port master

3.5.3 Interrupt controller (INTC)

The MCU implements an interrupt controller that features the following:

- Unique 9-bit vector for each of the 231 separate interrupt sources
- 8 software triggerable interrupt sources
- 16 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Ability to modify the ISR or task priority
- External high priority interrupt directly accessing the main core critical interrupt mechanism

3.5.4 System integration unit lite (SIUL)

The SIUL features the following:

- Up to 4 levels of internal pin multiplexing, allowing exceptional flexibility in the allocation of device functions for each package
- Centralized general purpose input output (GPIO) control of up to 149 input/output pins (package dependent)
- All GPIO pins independently configurable to support pull-up, pull down, or no pull
- Reading and writing to GPIO supported both as individual pins and 16-bit wide ports
- All peripheral pins can be alternatively configured as both general purpose input or output pins except ADC channels which support alternative configuration as general purpose inputs, with selected pins able to also support outputs
- Direct readback of the pin value supported on all digital output pins through the SIUL
- Configurable digital input filter that can be applied to up to 24 general purpose input pins for noise elimination on external interrupts

- Register configuration protected against change with soft lock for temporary guard or hard lock to prevent modification until next reset
- Support for two 32-bit virtual ports via the DSPI serialization

3.5.5 Flash memory

The MCU's on-chip flash memory features the following:

- Up to 1.5 MB burst flash memory
  - 4 × 128-bit page buffers with programmable prefetch control
  - Typical flash-memory access time: 0 wait-state for buffer hits, 2 wait-states for page buffer miss at 64 MHz
  - Page buffers can be allocated for code-only, fixed partitions of code and data, all available for any access
  - 64-bit ECC with single-bit correction, double-bit detection for data integrity
- Censorship protection scheme to prevent flash-memory content visibility
- Separate dedicated Data Flash for EEPROM emulation
  - 4 erase sectors each containing 16 KB of memory
  - Offers read-while-write functionality from main program space
- Small block flash-memory arrangement in main array to support features such as boot block, operating system block
- Hardware managed flash memory writes, erase and verify sequence
- Error correction status
  - Configurable error-correcting codes (ECC) reporting for SRAM and flash memory
  - Supports optional reporting of single-bit errors
  - Protected mechanism for reporting of corrected ECC values
  - Error address recorded including Access type and Master
  - Flash-memory ECC reporting registers mirrored into ECSM address space but data comes from the flash-memory module
  - Flash-memory module can be interrogated to provide ECC bit error location
  - Margin read for flash-memory array supported for initial program verification

3.5.6 SRAM

The MCU's on-chip SRAM features the following:

- Up to 96 KB general purpose SRAM
- Typical SRAM access time: 0 wait-state for reads and 32-bit writes; 1 wait-state for 8- and 16-bit writes if back to back with a read to same memory block
- 32-bit ECC with single-bit correction, double-bit detection for data integrity
- Supports byte (8-bit), half word (16-bit), and word (32-bit) writes for optimal use of memory

- User transparent ECC encoding and decoding for byte, half word, and word accesses
- Separate internal power domain applied to 32 KB SRAM block or 8 KB SRAM block during STANDBY modes to retain contents during low-power mode

3.5.7 Memory protection unit (MPU)

The MPU provides the following features

- 8 region descriptors for per-master protection
- Start and end address defined with 32-byte granularity
- Overlapping regions supported
- Protection attributes can optionally include process ID
- Protection offered for 3 concurrent read ports
- Read and write attributes for all masters
- Execute and supervisor/user mode attributes for processor masters

3.5.8 Boot assist module (BAM)

The device implements a Boot Assist Module (BAM):

- Block of read-only memory containing VLE code which is executed according to boot mode of the device
- Download of code into internal SRAM possible via FlexCAN or LINFlex, after which code can be executed

3.5.9 Enhanced modular input output system (eMIOS)

The chip implements a scaled-down version of the eMIOS module:

- Up to 64 timed I/O channels with 16-bit counter resolution
- Buffered updates
- Support for shifted PWM outputs to minimize occurrence of concurrent edges
- Supports configurable trigger outputs for ADC conversion for synchronization to channel output waveforms
- Edge-aligned output pulse width modulation
  - Programmable pulse period and duty cycle
  - Supports 0% and 100% duty cycle
  - Shared or independent time bases
- DMA transfer support available

3.5.10 Deserial serial peripheral interface module (DSPI)

The DSPI features the following:

- Up to 6 DSPI modules supported

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits
- Up to 6 chip select lines available, depending on package and pin multiplexing, to enable 64 external devices to be selected using external muxing from a single DSPI
- Up to 8 transfer types, independently configurable for each DSPI using the clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for deglitching
- FIFOs for buffering up to 4 transfers on the transmit and receive side
- General purpose I/O functionality on pins when not used for SPI
- Queueing operation possible through use of eDMA
- 32-bit serialization of data enabling virtual GPIO ports on 2 DSPI modules

3.5.11 Controller area network module (FlexCAN)

The enhanced FlexCAN module features the following:

- Up to 6 FlexCAN modules supported
- Compliant with CAN protocol specification, version 2.0B active
- 64 mailboxes per FlexCAN module
  - Mailboxes configurable while module remains synchronized to CAN bus
  - Each mailbox configurable as transmit or receive
- Transmit features
  - Supports configuration of multiple mailboxes to form message queues of scalable depth
  - Arbitration scheme according to message ID or message buffer number
  - Internal arbitration to guarantee no inner or outer priority inversion
  - Transmit abort procedure and notification
- Receive features
  - Individual programmable filters for each mailbox
  - 8 mailboxes configurable as a 6-entry receive FIFO
  - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
  - System clock
  - Direct oscillator clock to avoid PLL jitter
- Listen-only mode capabilities

- CAN sampler available for connection to one of available CAN module pads
  - Supports capturing of first message identifier while in STOP or STANDBY modes

3.5.12 System clocks and clock generation

The following list summarizes the system clock and clock generation on the MPC5607B:

- System clock can be derived from the following sources
  - External crystal oscillator
  - FMPLL
  - 16 MHz fast internal RC oscillator
- Programmable output clock divider of system clock (÷1, ÷2, ÷4)
- Separate programmable peripheral bus clock divider ratio (÷1, ÷2, ÷4) applied to system clock
- Frequency modulated phase-locked loop (FMPLL)
  - Input clock frequency from 4 MHz to 16 MHz
  - Clock source: external oscillator
  - Lock detect circuitry continuously monitors lock status
  - Loss of clock (LOC) detection for reference and feedback clocks
  - On-chip loop filter
    - Improves electromagnetic interference performance
    - Reduces number of external components required
- On-chip fast external crystal oscillator (FXOSC) supporting 4 MHz to 16 MHz
- Dedicated 16 MHz fast internal RC oscillator (FIRC)
  - Used as default clock source out of reset
  - Provides clock for rapid startup from low-power modes
  - Provides back-up clock in the event of FMPLL or external oscillator clock failure
  - Offers independent clock source for the watchdog timer
  - 5% accuracy over the operating temperature range
  - Trimming registers to support frequency adjustment with in-application calibration
- Dedicated 128 kHz slow internal RC oscillator (SIRC) for low-power mode operation and self wakeup
  - 10% accuracy
  - Trimming registers to support improve accuracy with in-application calibration
- 32 KHz slow external crystal oscillator (SXOSC) for low-power real-time clock

3.5.13 System timers

The system timers include:

- Periodic interrupt timer (PIT) timers (including ADC trigger)
- 1 Real-time counter (RTC) timer

The PIT is an array of timers that can be used to raise interrupts, trigger CTU channels, and ADC conversions. The RTC supports wakeup from low-power modes or real-time clock generation.

3.5.13.1 Periodic interrupt timer module (PIT)

The PIT features the following:

- 8 general purpose interrupt timers
- Up to 2 interrupt timers for triggering ADC injected conversions (one for 10-bit ADC, one for 12-bit ADC)
- Up to 4 interrupt timers for triggering DMA transfers
- Up to 2 interrupt timers for triggering CTU
- 32-bit counter resolution
- Clocked by system clock frequency

3.5.13.2 Real-time counter (RTC)

The RTC features the following:

- Configurable resolution for different timeout periods
  - 1 sec resolution for > 1 hour period
  - 1 ms resolution for 2 second period
- Selectable clock sources
  - 32 KHz slow external crystal oscillator (SXOSC)
  - 128 kHz slow internal RC oscillator (SIRC)
  - Divided 16 MHz fast internal RC oscillator (FIRC)
- Supports continued operation through all resets except POR (power-on reset)

3.5.14 System watchdog timer (SWT)

The watchdog on the MPC5607B features the following:

- Activation by software or out of reset
- 32-bit modulus counter
- Clock source: robust 128 kHz slow internal RC oscillator (divisible by 1 to 32)
- Supports normal or windowed mode
- Configurable response on timeout: reset, interrupt, or interrupt followed by reset
- Reset by writing a software key to memory mapped register
- Support for protected access to watchdog control registers with optional soft and hard locks
  - Soft lock allows temporary locking of configuration
  - Once enabled, hard lock prevents any changes until after a reset
- Supports halting during low-power modes

3.5.15 Inter-integrated circuit (I^2C) module

The I^2C module features the following:

- 1 I^2C module supported
- 2-wire bidirectional serial bus for on-board communications
- Compatibility with I^2C bus standard
- Multimaster operation
- Software-programmable for one of 256 different serial clock frequencies
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

3.5.16 On-chip voltage regulator (VREG)

The on-chip voltage regulator includes the following features:

- Optional support for internal and external ballast resistor based on power consumption
- Regulates 3.3 or 5 V ±10% input to generate all internal supplies for internal control
- Manages power gating
- Low-power regulators support operation when in STOP and STANDBY modes to minimize power consumption
- Fast startup on-chip regulators for rapid exit from low-power modes
- Low voltage reset supported on all internal supplies

3.5.17 Analog-to-digital converter (ADC)

The ADC features the following:

- 2 ADC modules, one 10-bit resolution and one 12-bit resolution supporting synchronous conversions on channels
- 0–V_{DD} common mode conversion range
- Independent reference supplies for each ADC
- Conversions times of < 1 µs available
- Up to 53 single ended inputs channels, expandable to 81 channels with external multiplexers
- Up to 19 shared channels, among which, 16 called ANP are mapped on dedicated pins, not multiplexed with any other functionality, in order to improve the accuracy. All other channels, called ANS or ANX are multiplexed with other functionalities.

  - Up to 19 channels shared between 10-bit and 12-bit ADCs
  - Up to 5 dedicated 12-bit ADC channels
  - Up to 29 dedicated 10-bit ADC channels
- Externally multiplexed channels
  - Internal control to support generation of external analog multiplexor selection
  - 4 internal channels optionally used to support externally multiplex inputs, providing transparent control for additional ADC channels
  - Each of the 3 channels supports up to 8 externally muxed inputs
  - Individual dedicated result register also available for externally muxed conversion channels
  - 3 independently configurable sample and conversion times for high occurrence channels, internally muxed channels and externally muxed channels
- Configurable right-aligned or left-aligned result formats
- Support for one-shot, scan and injection conversion modes
- Independently configurable parameters for channels:
  - Offset refresh
  - Sampling
- Conversion triggering support
  - Internal conversion triggering from periodic interrupt timer (PIT) or timed I/O module (eMIOS) through cross triggering unit (CTU)
  - Internal conversion triggering from periodic interrupt timer (PIT)
  - 1 input pin configurable as external conversion trigger source
- Up to 6 configurable analog comparator channels offering range comparison with triggered alarm
  - Greater than
  - Less than
  - Out of range
- All unused analog pins available as general purpose input pins
- Unused 10-bit ADC analog pins, with the exception of the 19 dedicated high accuracy channels, available as general purpose output pins
- Power-down mode
- Supports DMA transfer of results based on end of conversion chain or each conversion
- Separate dedicated DMA request for injection mode

3.5.18 Enhanced direct memory access controller (eDMA)

The following summarizes the chip's implementation of the eDMA controller:

- 16 channels to support independent 8, 16, or 32-bit single value or block transfers
- Support of variable sized queues and circular queues
- Source and destination address registers independently configured to post-increment or remain constant

- Each transfer initiated by peripheral, CPU, periodic timer interrupt or eDMA channel request
- Peripheral DMA request sources possible from SPIs, I^2C, 10-bit ADC, 12-bit ADC, eMIOS and GPIOs
- Each eDMA channel able to optionally send interrupt request to CPU on completion of single value or block transfer
- DMA transfers possible between system memories and all accessible memory mapped locations including peripheral and registers
- Programmable DMA Channel Mux allows assignment of any DMA source to any available DMA channel with total of up to 64 potential request sources

3.5.19 Cross trigger unit (CTU)

The CTU enables the synchronization of ADC conversions with a timer event. Its key features are:

- Single cycle delayed trigger output trigged by up to 64 input flags/events connected to different timers in the system
- Triggers ADC conversions from any eMIOS channel
- Triggers ADC conversions from up to 2 dedicated PITs
- Maskable interrupt generation whenever a trigger output is generated
- 1 event configuration register dedicated to each timer event allows to define the corresponding ADC channel
- Acknowledgment signal to eMIOS/PIT for clearing the flag
- Synchronization with ADC to avoid collision

3.5.20 Serial communication interface module (LINFlex)

The LINFlex on the MPC5607B features the following:

- Up to 10 LINFlex modules supported
- Supports LIN master mode, LIN slave mode and UART mode
- DMA connected on LINFlex_0 and LINFlex_1
- LINFlex_0 supporting LIN master and slave mode; LINFlex_1 to LINFlex_9 modules supporting LIN master mode
- LIN state machine compliant to LIN 1.3, 2.0 and 2.1 specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
  - Autonomous LIN frame handling
  - Message buffer to store identified and up to 8 data bytes
  - Supports message length of up to 64 bytes
  - Detection and flagging of LIN errors
    - Sync field
    - Delimiter

  - ID parity
  - Bit, framing
  - Checksum and timeout errors
- Classic or extended checksum calculation
- Configurable break duration of up to 36-bit times
- Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
- Diagnostic features
  - Loop back
  - Self Test
  - LIN bus stuck dominant detection
- Interrupt driven operation with 16 interrupt sources

- LIN slave mode features
  - Autonomous LIN header handling
  - Autonomous LIN response handling
  - 16 identifiers filters for discarding irrelevant LIN frames
- UART mode
  - Full-duplex operation
  - Standard non return-to-zero (NRZ) mark/space format
  - Data buffers with 4-bytes receive, 4-bytes transmit
  - Configurable word length (8-bit or 9-bit words)
  - Error detection and flagging
    - Parity, noise and framing errors
  - Interrupt driven operation with 4 interrupt sources
  - Separate transmitter and receiver CPU interrupt sources
  - 16-bit programmable baud rate modulus counter and 16-bit fractional
  - 2 receiver wakeup methods

MPC5607B devices include two functionally different LINFlex controller types. These are distinguished in the documentation by the abbreviations “LINFlex” and “LINFlexD”. The latter name represents the DMA support available on this controller type. The MPC5607B devices combine these two types to provide up to 10 modules supporting the LINFlex protocol. Table 4 shows the module (instance) numbers and the corresponding functional controller type.

Table 4. LINFlex numbering and naming

Module numbers	Module version
0 and 1	LINFlexD
2–9	LINFlex

3.5.21 Nexus port controller (NPC)

Nexus features the following:

- According to IEEE-ISTO 5001-2003
- Nexus 2+ features supported
  - Static debug
  - Watchpoint messaging
  - Ownership trace messaging
  - Program trace messaging
  - Real-time read/write of any internally memory mapped resources through JTAG pins
  - Overrun control, which selects whether to stall before Nexus overruns or keep executing and allow overwrite of information
  - Watchpoint triggering, watchpoint triggers program tracing
- Configured via the IEEE 1149.1 (JTAG) port
- Nexus auxiliary port supported on 208 MAPBGA packages

3.5.22 JTAG controller (JTAGC)

JTAG features the following:

- JTAG low pin count interface (IEEE 1149.1) test access port (TAP) interface
- Backward compatible to standard JTAG IEEE 1149.1-2001 test access port (TAP) interface
- Supports boundary scan testing
- All JTAG pins reusable in application as standard IOs

3.6 Packages

MPC5607B family members are offered in the following package types:

- 100-pin LQFP, 0.5 mm pitch, 14 mm × 14 mm outline
- 144-pin LQFP, 0.5 mm pitch, 20 mm × 20 mm outline
- 176-pin LQFP, 0.5 mm pitch, 24 mm × 24 mm outline
- 208-ball MAPBGA, 1 mm ball pitch, 17 mm × 17 mm outline

4 Developer environment

The MPC5607B MCU family is supported by tools and third-party developers similar to those supporting Freescale MPC5500 products, offering a widespread, established network of tools and software vendors. The MPC5607B MCU also features a high-performance Nexus debug interface.

The following development support is available:

- Automotive evaluation boards (EVB) featuring CAN, LIN interfaces, and more
- Compilers

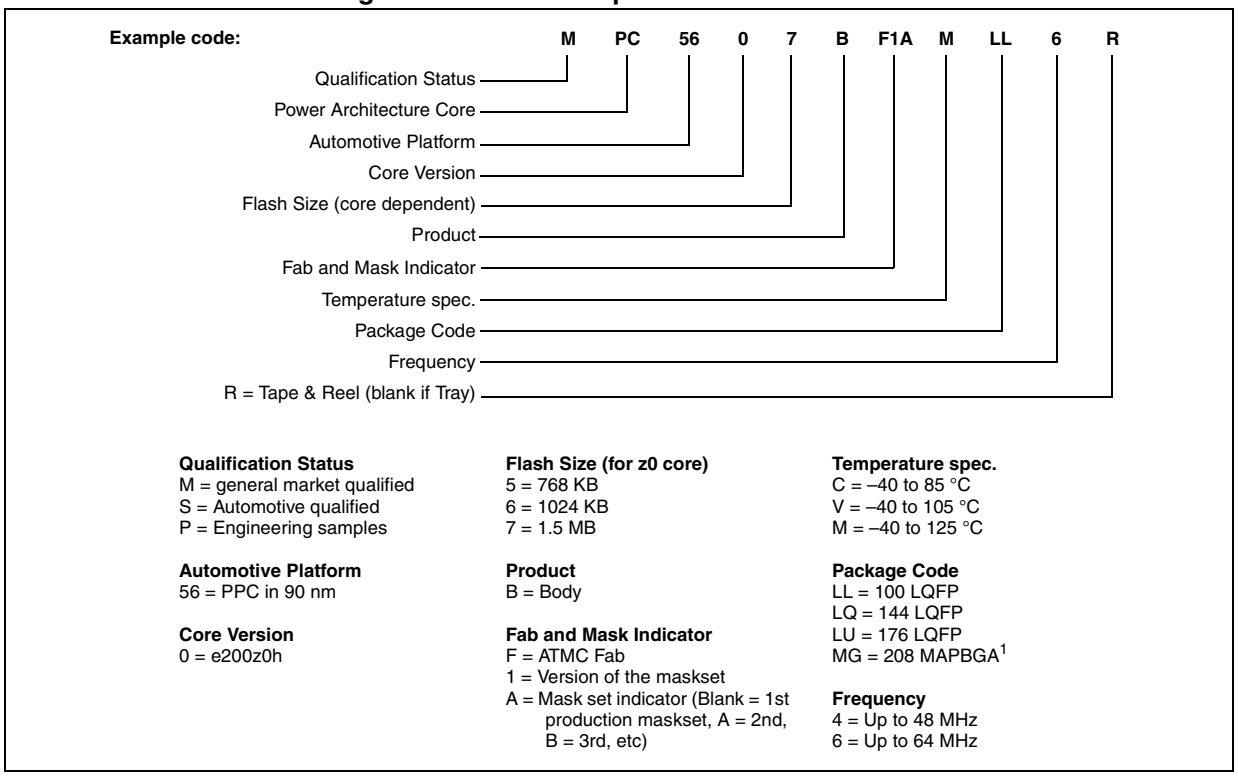
- Debuggers
- JTAG and Nexus interfaces

The following software support is available:

- OSEK solutions is available from multiple third parties
- CAN and LIN drivers
- AUTOSAR package

5 Orderable parts

Figure 3. Commercial product code structure



1 208 MAPBGA available only as development package for Nexus2+

6 Revision history

Table 5 summarizes revisions to this document.

Table 5. Document revision history

Revision	Date	Substantive changes
1	5/2008	Initial release

Table 5. Document revision history (continued)

Revision	Date	Substantive changes
2	29-Oct-2008	Made minor editing and formatting changes to improve readability Replaced “e200z0” with “e200z0h” throughout document Section 4, Device family overview: Reorganized chapter Table 2: - Replaced OPWFMBC with OPWFMB / OPWMCB in eMIOS channel type - Updated eMIOS channel counts and GPIO pin counts - Modified footnotes 7 and 8 Section 4.3, Critical performance parameters: - Replaced “-40 to 150 °C junction temperature” with “-40 to 125 °C ambient operating temperature range” - Replaced “ballast control” with “ballast resistor” Updated Table 3, Table 4 and Table 7; changed V_{DDE} from 5.5 V to 5.0 V for Table 5 Section 4.4, Low power operation: - Reorganized content presentation - Modified second paragraph to state that the STANDBY mode, not the STOP mode, uses power gating - Changed pins available for wakeup from STANDBY from “24 I/O” to “23 external wakeup” - Changed RAM retained in STANDBY2 mode from “full contents” to “32 KB” - Replaced “up to 18 external pins” with “up to 23 external wakeup pins” in last sentence
2 (continued)	29-Oct-2008 (continued)	Section 4.5, Chip-level features: - Replaced “Up to 6” with “8” PITs - Specified number of ADCs as 2 Section 4.6.2, e200z0h core processor: Replaced “Thirty-two 32-bit general purpose registers (GPRs)” with “32-bit general purpose registers (GPRs)” Table 8: Removed shadow block row Section 4.6.7, SRAM: Replaced “full RAM block and 8” with “32 Kbyte RAM block or 8” in last bullet Table 9: - Replaced “OPWFMCB” with “OPWFMB / OPWMCB” in channel type header - Replaced “-x” with “x” for mode “MCB” in column “O(I)PWM / OPWFMB / OPWMCB / ICOC” Table 10: - Replaced “OPWFMCB” with “OPWFMB / OPWMCB” in channel type - Modified footnotes 3 and 4

Table 5. Document revision history (continued)

Revision	Date	Substantive changes
2 (continued)	29-Oct-2008 (continued)	Section 4.6.12, Controller Area Network Module (FlexCAN): Modified CAN sampler subfeature at end of section Section 4.6.13, System clocks and clock generation: - Removed internal 16 MHz RC oscillator as FMPLL clock source - Changed accuracy of 128 kHz RC oscillator from 5% to 10% Section 4.6.14.1, Introduction: Updated second paragraph Section 4.6.14.2, Periodic interrupt timer module (PIT): - Replaced “Up to 6” with “8” GP interrupt timers - Updated triggering features Section 4.6.15, System watchdog timer: Updated Section 4.6.17, On-chip voltage regulator (VREG): - Replaced “ballast transistor” with “ballast resistor” - Replaced “external ballast only” with “external ballast resistor only” - Modified input voltage range Section 4.6.18, Analog to Digital Converter Module (ADC): - Updated feature description for unused 10-bit ADC analog pins - Updated conversion triggering support features - Removed injection mode status bit and associated subbullets from feature list Section 4.6.20, Cross Trigger Unit (CTU): Modified description for triggering of ADC conversions from PITs Section 4.6.21, Serial Communication Interface Module (LINFlex): Removed DMA support capability Section 4.6.23, JTAG controller (JTAGC): Added bullet “All JTAG pins reusable in application as standard IOs” Section 5, Developer environment: Removed standard reconfiguration routines from software support bullets Added Section 6, Order codes
3	05-Nov-2008	No substantive changes between Rev. 2 and Rev. 3.
4	30-Oct-2009	In the features section: • Updated external IRQs. • Added DMA capability for LinFlex. • Revised the low power standby mode. • Revised the ADC features. In the family comparison table: • Moved package row to beginning of table. • Replaced N2P with N2+ . • Revised the ADC information. • Removed “10-bit/12-bit ADC” info (it is already reflected individually in other entries).
5	25-Jan-2010	Editorial changes and improvements. Revised the block diagram to match the diagram used in other MPC5607B documents. Added the “MPC5607B series block summary” table. Revised the “Module features” section to match those used in other MPC5607B documents.

Table 5. Document revision history (continued)

Revision	Date	Substantive changes
6	19-Apr-2010	Throughout the document: • Replaced “RAM” with “SRAM” • Replaced “DMA“ with “eDMA“ In the block diagram figure: • Replaced “CAN” with “FlexCAN” in the legend • Added the “5ch 12-bit ADC“ block • Added “eDMA” in the legend In the “Analog-to-Digital Converter (ADC)“ section: • Updated the total number of the single-ended input channels (was 48) and thus the total number of the channels also considering the expandable ones (was 92) • Changed the specifications about the shared and dedicated channels as for 10-bit and 12-bit ADC In the “Orderable part number summary“ table: • Removed the E after 560xB for all of the parts Inserted commercial product code structure.
7	26-Aug-2010	Removed “Current consumption estimates” table Removed second level bullet from “Interrupt Controller (INTC)” section Removed “Flash partitioning” table Rewrote first bullet within “Cross Trigger Unit (CTU)” section Updated the “Serial Communication Interface Module (LINFlex)” section Removed “P/I” from the blocks of “Body controller application example” figure Removed “Order code” table Replaced “e200z0” with “e200z0h” into commercial product code structure.
8	15-Jul-2011	Formatting and editorial changes throughout Reorganized content of introduction Device block diagram: added GPIO and VREG to legend Device block summary table: • changed “System watchdog timer” to “Software watchdog timer” • in WKPU function, changed “up to 18 external sources” to “up to 27 external sources” Device family comparision table: • changed LINFlex count for 144-pin LQFP—was ‘6’; is ‘8’ • changed LINFlex count for 176-pin LQFP—was ‘8’; is ‘10’ Section “Critical performance parameters”: • removed tables “I/O characteristics, V_{DDE} = 5.0 V”, “I/O characteristics, V_{DDE} = 3.3V”, and “FMPLL characteristics” (this information can be found in the chip datasheet) • changed “105 °C” to “125 °C” as T_A for operation at 64 MHz Section “Low-power operation”: changed “from STANDBY mode by any of up to 23 external wakeup pins” to “from STANDBY mode by any of up to 27 external wakeup pins” Section “System integration unit lite (SIUL)”: changed “up to 16 general purpose input pins” to “up to 24 general purpose input pins” Section “Enhanced modular input output system (eMIOS)”: removed tables “Supported eMIOS channel modes” and “eMIOS configuration” (this information can be found in the chip reference manual) Section “Software watchdog timer (SWT)”: changed title (was “System watchdog timer”)

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