LTC6948

Ultralow Noise and Spurious Fractional-N Synthesizer with Integrated VCO

DESCRIPTION

Demonstration circuit 1959B features the LTC6948, an Ultralow Noise and Spurious Fractional-N Synthesizer with Integrated VCO.

There are four options of the DC1959B, one for each version of the LTC6948. Table 1 summarizes the available DC1959B options.

The DC1959B provides 50Ω SMA connectors for the reference frequency input f_{REF} (REF+IN) and the differential RF output (RF+ and RF–).

A DC590 USB serial controller board is used for SPI communication with the LTC6948, controlled by the supplied FracNWizard™ software.

Design files for this circuit board are available at http://www.linear.com/demo/DC1959B
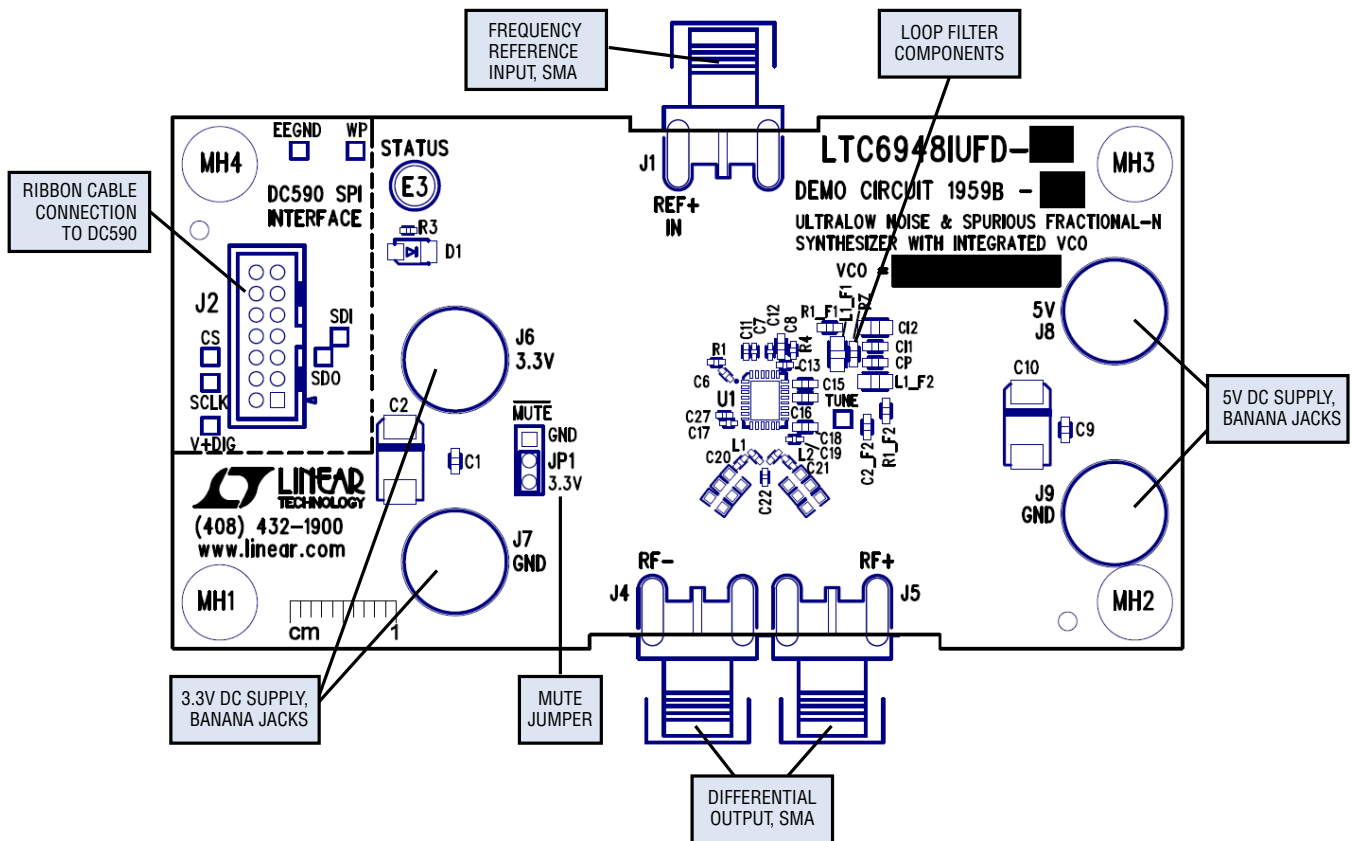
Figure 1. DC1959B Connections

QUICK START PROCEDURE

The DC1959B is easy to set up to evaluate the performance of the LTC6948. Follow the procedure below.

The DC590 and FracNWizard application are required to control the DC1959B through a personal computer (PC).

DC590 Configuration

Place the DC590 jumpers in the following positions (refer to Figure 2):

JP4: EE – Must be in the EN position.

JP5: ISO – ON must be selected.

JP5: SW – ON must be selected.

JP6: VCCIO – 3.3V must be selected. This sets the SPI port to 3.3V operation.

Connect the DC590 to one of your computer's USB ports with the included USB cable.

FracNWizard Installation

The FracNWizard software is used to communicate with the LTC6948 synthesizer. It uses the DC590 to translate between USB and SPI-compatible serial communications formats. It also includes advanced PLL design and simulation capabilities. The following are the FracNWizard system requirements:

- Windows Operating System: Windows XP, Windows 2003 Server, Windows Vista, Windows 7

- Microsoft .NET 3.5 SP1 or later

- Windows Installer 3.1 or later

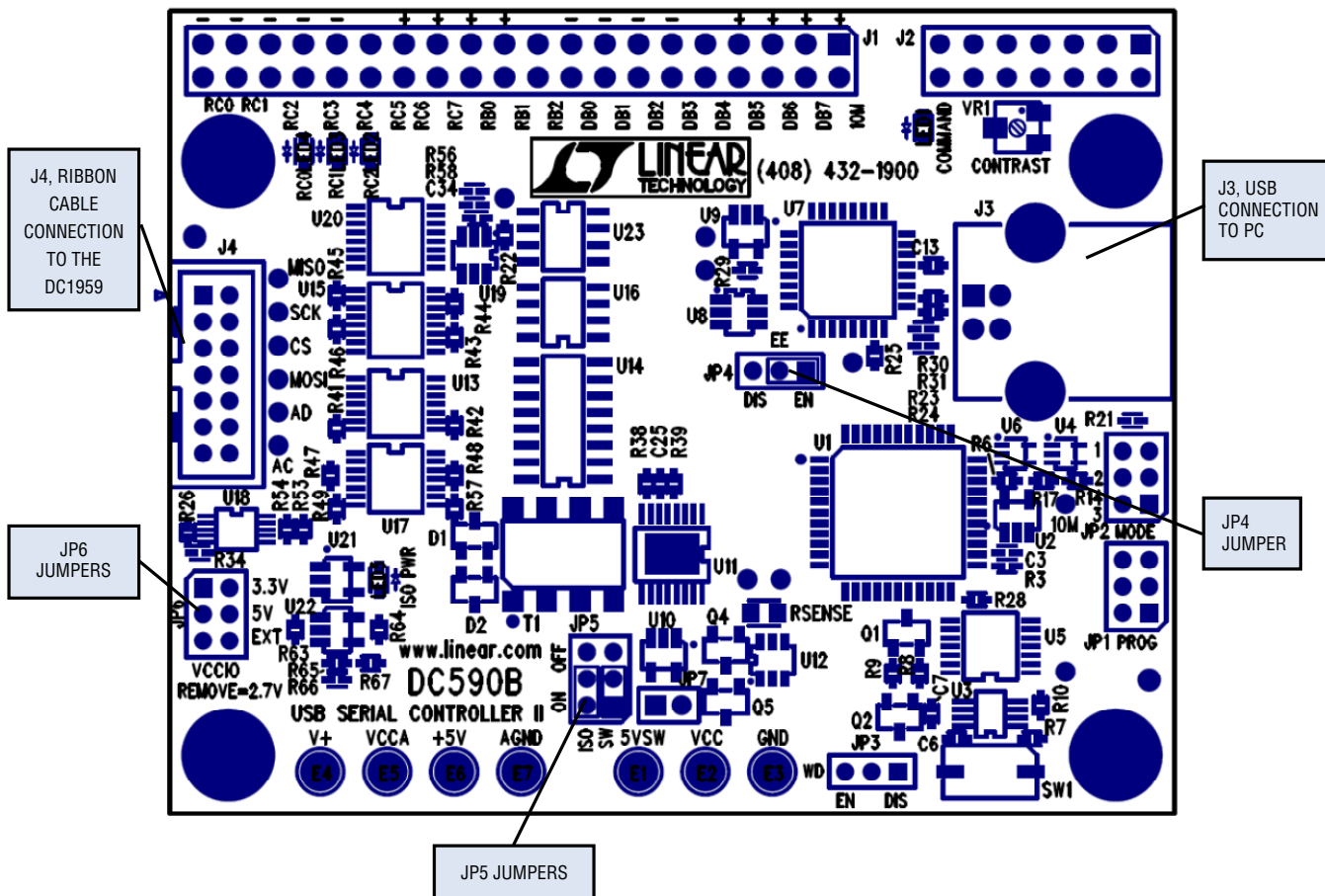- Linear Technology's DC590 hardware

Figure 2. DC590 Jumper and Connector Locations

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QUICK START PROCEDURE

Download the FracNWizard setup file at www.linear.com/FracNWizard.

Run the FracNWizard setup file and follow the instructions given on the screen. The setup file will verify and/or install Microsoft .NET and install the FracNWizard. Refer to the Help menu for software operation.

DC1959B Configuration

1. Connect a 100MHz reference frequency source to REF+IN (at J1) and signal analyzers to RF+ and/or RF– (at J5 and/or J4) using the SMA connectors (see Figure 1 and the Typical DC1959B Requirements and Characteristics table).

   Be sure to terminate any unused RF output with 50Ω, or poor spurious performance may result.

2. Choose the $\overline{\text{MUTE}}$ jumper setting:

JP1: GND/3.3V – $\overline{\text{MUTE}}$ position. Select GND to mute the RF output, 3.3V to un-mute.

3. Connect the GND, 3.3V, and 5V banana jacks to a power supply and apply power (see Figure 1 and the Typical DC1959B Requirements and Characteristics table).

4. Connect the DC590 to the DC1959B with the provided ribbon cable.

5. Run the FracNWizard application.

6. In FracNWizard, click File -> Load Settings and point to the LTC6948-1_100MHz.fracnset file in case of evaluating the LTC6948-1, for instance, or load the appropriate file depending on which option of the LTC6948 you are evaluating.

The red LED on the DC1959B should turn on indicating that the loop is locked and the output is at 907MHz.
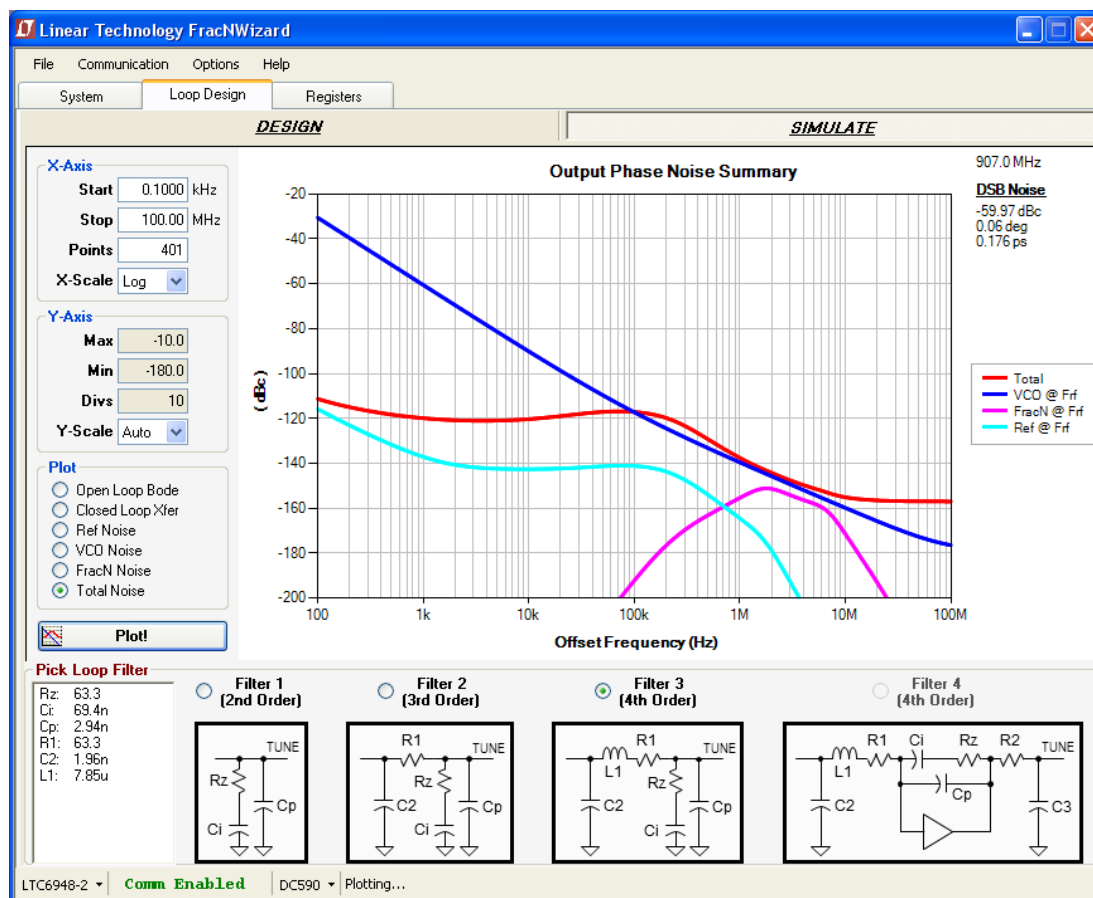

Figure 3. FracNWizard Screenshot

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QUICK START PROCEDURE

Troubleshooting

If the red LED does not illuminate, follow the instructions below:

1. Verify that you are able to communicate with the DC1959B. The bottom status line in FracNWizard should read LTC6948 and Comm Enabled as shown in Figure 3. Refer to FracNWizard's Troubleshoot and Help if not.

2. Verify that the 3.3V and 5V have the correct voltages on them and that the reference frequency is applied to the REF+IN SMA input.

If the red LED is on but you cannot detect an RF output, make sure jumper JP1 is at the 3.3V position. Run Help -> Troubleshoot in FracNWizard if the problem is not resolved.

DC1959B Reconfiguration

You can redesign the frequency plan of the DC1959B using FracNWizard. You can change the loop filter as found using FracNWizard by reinstalling the loop filter components shown in Figure 1.

ASSEMBLY OPTIONS

Table 1. DC1959B Options and Frequency Ranges

ASSEMBLY VERSION	PART NUMBER	VCO FREQUENCY RANGE (GHz)	OUTPUT DIVIDER SETTINGS
DC1959B-A	LTC6948IUFD-1	2.240 to 3.740	Integers 1 through 6
DC1959B-B	LTC6948IUFD-2	3.080 to 4.910	Integers 1 through 6
DC1959B-C	LTC6948IUFD-3	3.840 to 5.790	Integers 1 through 6
DC1959B-D	LTC6948IUFD-4	4.200 to 6.390	Integers 1 through 6

TYPICAL DC1959B REQUIREMENTS AND CHARACTERISTICS

| PARAMETER	INPUT OR OUTPUT	PHYSICAL LOCATION	DETAILS
3.3V Power Supply	Input	J6 and J7 Banana Jacks	Low-Noise and Spur-Free 3.3V, 130mA
5V Power Supply	Input	J8 and J9 Banana Jacks	Low-Noise and Spur-Free 5V, 33mA
REF+ IN, Reference Frequency	Input	J1 SMA Connector	Low-Noise 100MHz*, 6dBm to 10dBm into 50Ω, See Note Below
RF+ and RF–	Two Outputs	J4 and J5 SMA Connectors**	Frequency: 907MHz*, Power: 0dBm, Frequency Range: Depends on the Version of the LTC6948 Device – Refer to Table 1
Loop Bandwidth	–	Set by Loop Filter Component Values	Approximately 160kHz* Depending on the DC1959B Version

*These frequencies are for the DC1959B fracnset files included with FracNWizard.
**Any unused RF output must be terminated with 50Ω, or poor spurious performance may result.

Note: A low noise 100MHz reference frequency, such as the Wenzel 501-04516D OCXO, is recommended. If using a different frequency, make sure to update the Fref and R_DIV boxes under the System tab in FracNWizard so that Fpfd is still 50MHz. For example, if a 250MHz clock is used, Fref should be changed to 250MHz and R_DIV to 5. Ref BST and FILT under the System tab in FracNWizard might need to be changed if the reference frequency and/or power is different than what is recommended in the table above. More information can be found in the LTC6948 data sheet.

PCB LAYOUT

The top metal layer of the DC1959B is shown here as an example of good PCB layout for the LTC6948.
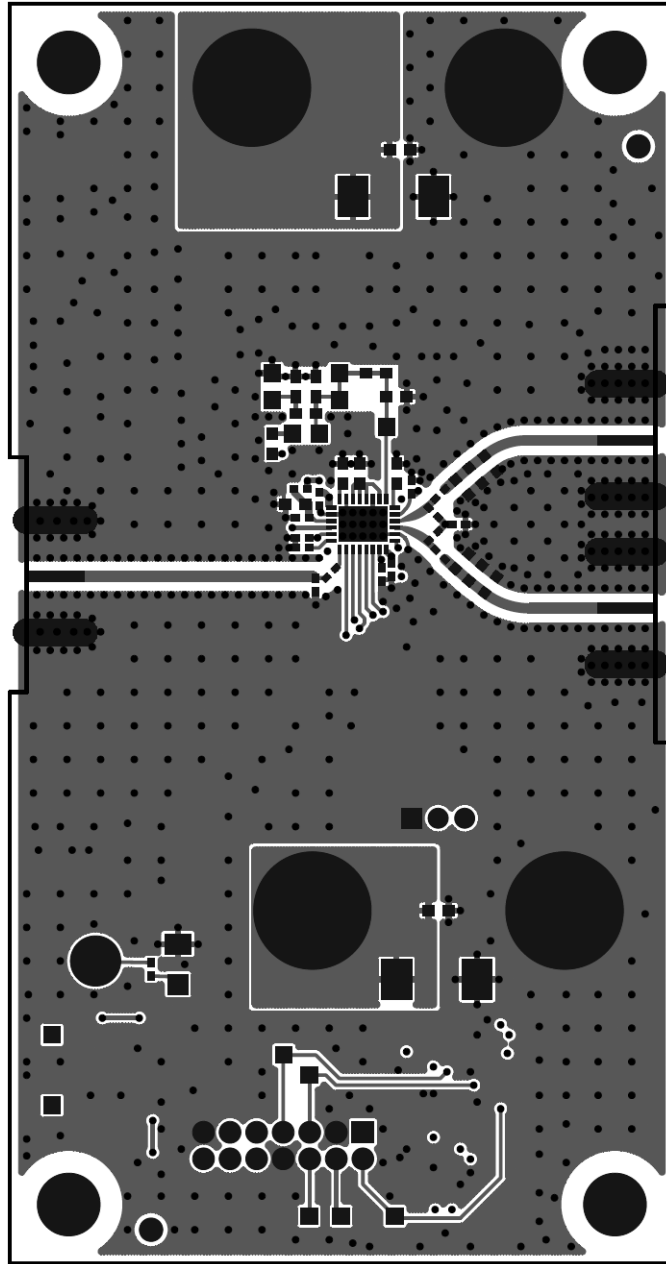
PARTS LIST

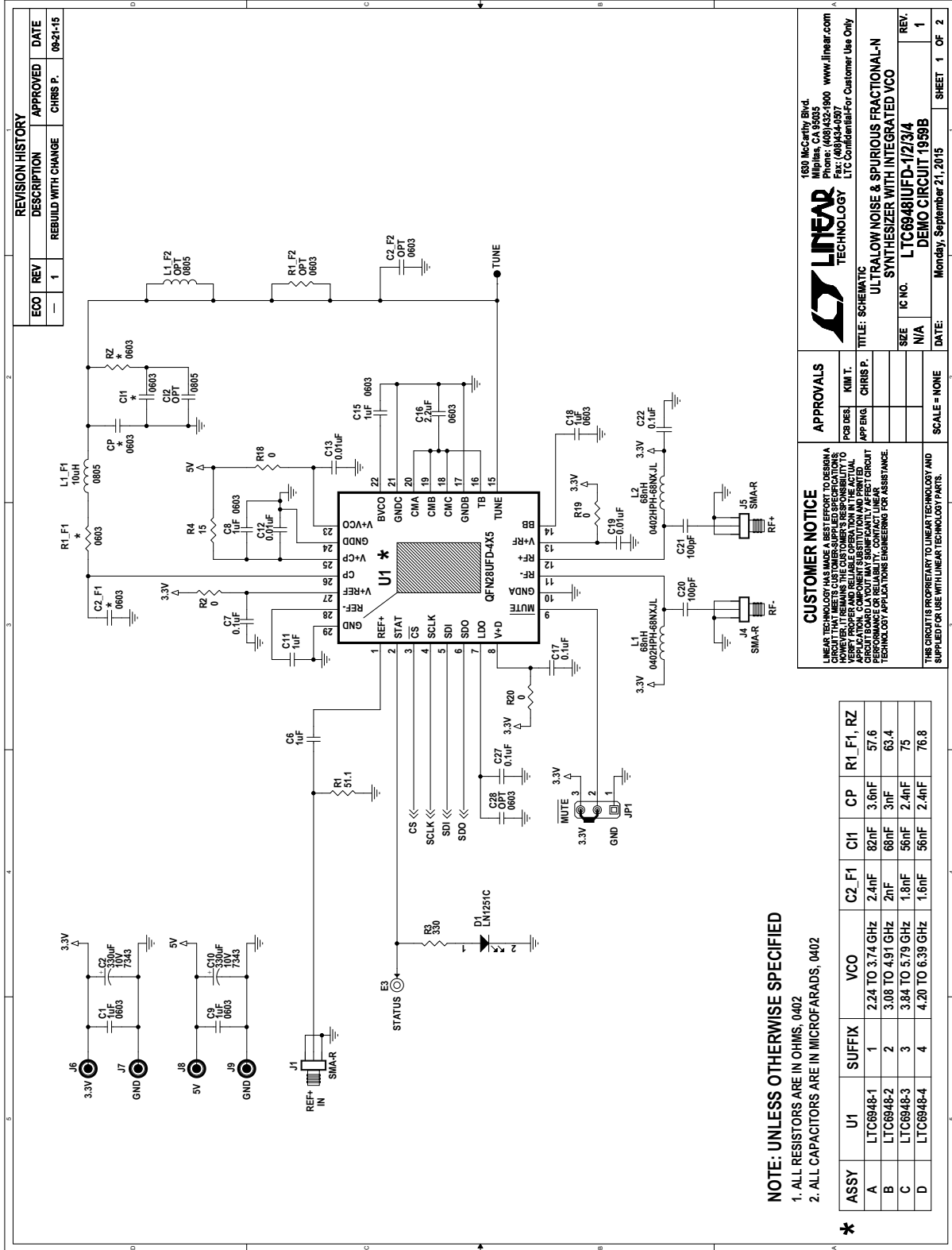| ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	0	CI2	CAP., 0805	OPT
2	5	C1, C8, C9, C15, C18	CAP., X7R, 1.0µF, 16V, 10%, 0603	TDK, C1608X7R1C105K
3	2	C2, C10	CAP., TANT., 330µF, 10V, 10%, 7343	AVX, TPME337K010R0035
4	9	C3, C7, C17, C22-C27	CAP., X7R, 0.1µF, 10V, 10%, 0402	TDK, C1005X7R1A104K
5	2	C6, C11	CAP., X5R, 1.0µF, 16V, 10%, 0402	TDK, C1005X5R1C105K
6	3	C12, C13, C19	CAP., X7R, 0.01µF, 16V, 10%, 0402	AVX, 0402YC103KAT2A
7	1	C16	CAP., X5R, 2.2µF, 16V, 10%, 0603	TDK, C1608X5R1C225K
8	0	C2_F2, C28	CAP., 0603	OPT
9	2	C20, C21	CAP., X7R, 100pF, 50V, 10%, 0402	AVX, 04025C101KAT2A
10	1	D1	LED, RED	PANASONIC, LN1251C-TR
11	1	E3	TURRET, TESTPOINT, 2501	MILL-MAX, 2501-2-00-80-00-00-07-0
12	1	JP1	HEADERS, 3 PINS 2mm CTRS.	SAMTEC, TMM-103-02-L-S
13	3	J1, J4, J5	CON., SMA 50Ω EDGE-LAUNCH	E.F. JOHNSON, 142-0701-851
14	1	J2	CON., HEADER, 14 PIN, 2mm	MOLEX, 87831-1420
15	4	J6, J7, J8, J9	JACK, BANANA	KEYSTONE, 575-4
16	2	L1, L2	IND., 68nH 5%, 0402	COILCRAFT, 0402HPH-68NXJLW
17	1	L1_F1	IND., 10µH, 0805	TDK, MLF2012E100K
18	0	L1_F2	IND., 0805	OPT
19	1	R1	RES., CHIP, 51.1Ω, 1/16W, 1%, 0402	NIC, NRC04F51R1TRF
20	0	R1_F2	RES., 0603	OPT
21	4	R2, R18, R19, R20	RES., CHIP, 0Ω, 0402	NIC, NRC04Z0TRF
22	1	R3	RES., CHIP, 330Ω, 1/16W, 1%, 0402	NIC, NRC04F3300TRF
23	1	R4	RES., CHIP, 15Ω, 1/16W, 1%, 0402	NIC, NRC04F15R0TRF
24	4	R5, R6, R7, R13	RES., CHIP, 200k, 1/16W, 1%, 0402	NIC, NRC04F2003TRF
25	3	R8, R9, R14	RES., CHIP, 4.99k, 1/16W, 1%, 0402	NIC, NRC04F4991TRF
26	3	R10, R11, R12, R21	RES., CHIP, 100Ω 1/16W, 5%, 0402	NIC, NRC04J101TRF
27	1	R15	RES., CHIP, 0Ω, 0603	NIC, NRC06Z0TRF
28	2	U2, U3	I.C., DUAL BUFFER, SC70-6	FAIRCHILD SEMI., NC7WZ17P6X
29	1	U4	I.C., DUAL TRANSCEIVER, SOT363	NXP, 74LVC1T45GW+125
30	1	U5	I.C., SERIAL EEPROM, TSSOP8	MICROCHIP, 24LC025-I /ST
31	1	SHUNT ON JP1	SHUNT, 2mm CTRS.	SAMTEC 2SN-BK-G

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
DC1959B-A Required Circuit Components				
1	1		DC1959B GENERAL BOM	
2	1	C2_F1	CAP., C0G, 2.4nF, 50V, 5%, 0603	MURATA, GRM1885C1H242JA01D
3	1	CI1	CAP., X7R, 82nF, 50V, 10%, 0603	MURATA, GRM188R71H823KA93D
4	1	CP	CAP., C0G, 3.6nF, 50V, 5%, 0603	MURATA, GRM1885C1H362JA01D
5	2	R1_F1, RZ	RES., CHIP, 57.6Ω, 1/16W, 1%, 0603	NIC, NRC06F57R6TRF
6	1	U1	I.C. SYNTHESIZER, QFN28UFD-4X5	LINEAR TECH., LTC6948IUFD-1
DC1959B-B Required Circuit Components				
1	1		DC1959B GENERAL BOM	
2	1	C2_F1	CAP., C0G, 2nF, 50V, 5%, 0603	MURATA, GRM1885C1H202JA01D
3	1	CI1	CAP., X7R, 68nF, 50V, 10%, 0603	MURATA, GRM188R71H683KA93D
4	1	CP	CAP., C0G, 3nF, 50V, 5%, 0603	MURATA, GRM1885C1H302JA01D
5	2	R1_F1, RZ	RES., CHIP, 63.4Ω, 1/16W, 1%, 0603	NIC, NRC06F63R4TRF
6	1	U1	I.C. SYNTHESIZER, QFN28UFD-4X5	LINEAR TECH., LTC6948IUFD-2
DC1959B-C Required Circuit Components				
1	1		DC1959B GENERAL BOM	
2	1	C2_F1	CAP., X7R, 1.8nF, 50V, 10%, 0603	MURATA, GRM188R71H182KA01D
3	1	CI1	CAP., X7R, 56nF, 50V, 10%, 0603	MURATA, GRM188R71H563KA93D
4	1	CP	CAP., C0G, 2.4nF, 50V, 5%, 0603	MURATA, GRM1885C1H242JA01D
5	2	R1_F1, RZ	RES., CHIP, 75Ω, 1/16W, 5%, 0603	VISHAY, CRCW060375R0JNEA
6	1	U1	I.C. SYNTHESIZER, QFN28UFD-4X5	LINEAR TECH., LTC6948IUFD-3
DC1959B-D Required Circuit Components				
1	1		DC1959B GENERAL BOM	
2	1	C2_F1	CAP., C0G, 1.6nF, 50V, 5%, 0603	MURATA, GRM1885C1H162JA01D
3	1	CI1	CAP., X7R, 56nF, 50V, 10%, 0603	MURATA, GRM188R71H563KA93D
4	1	CP	CAP., C0G, 2.4nF, 50V, 5%, 0603	MURATA, GRM1885C1H242JA01D
5	2	R1_F1, RZ	RES., CHIP, 76.8Ω, 1/16W, 1%, 0603	NIC, NRC06F76R8TRF
6	1	U1	I.C. SYNTHESIZER, QFN28UFD-4X5	LINEAR TECH., LTC6948IUFD-4

SCHEMATIC DIAGRAM

NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE IN OHMS, 0402
2. ALL CAPACITORS ARE IN MICROFARADS, 0402

ASSY	U1	SUFFIX	VCO	C2_F1	CI1	CP	R1_F1, RZ
A	LTC6948-1	1	2.24 TO 3.74 GHz	2.4nF	82nF	3.6nF	57.6
B	LTC6948-2	2	3.08 TO 4.91 GHz	2nF	68nF	3nF	63.4
C	LTC6948-3	3	3.84 TO 5.79 GHz	1.8nF	56nF	2.4nF	75
D	LTC6948-4	4	4.20 TO 6.39 GHz	1.6nF	56nF	2.4nF	76.8

REVISION HISTORY

ECO	REV	DESCRIPTION	APPROVED	DATE
—	1	REBUILD WITH CHANGE	CHRIS P.	09-21-15

APPROVALS

| PCB DES. | KIM T. |
| APP ENG. | CHRIS P. |

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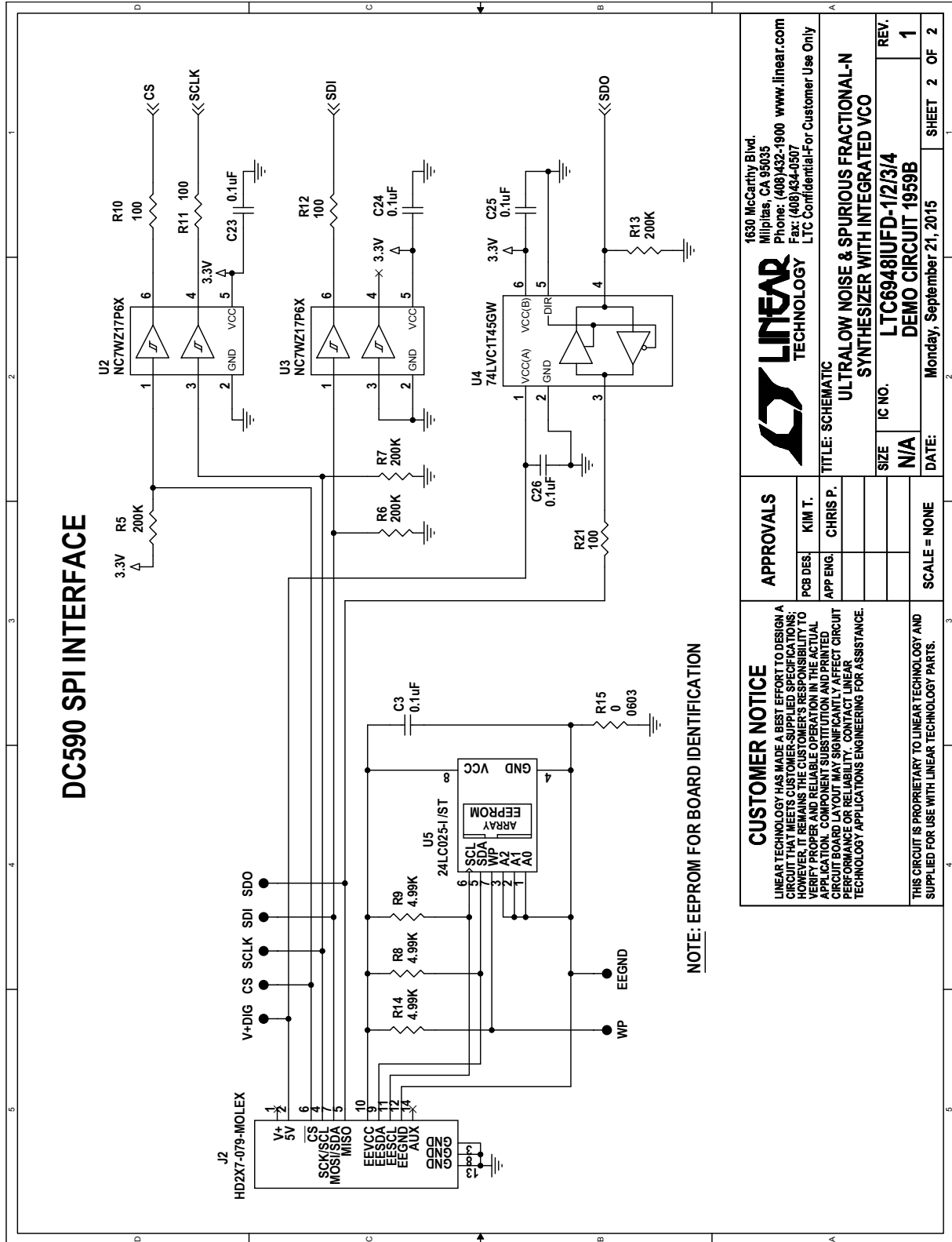Phone: (408)432-1900   www.linear.com
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TITLE: SCHEMATIC
ULTRALOW NOISE & SPURIOUS FRACTIONAL-N SYNTHESIZER WITH INTEGRATED VCO

IC NO.   LTC6948IUFD-1/2/3/4
DEMO CIRCUIT 1959B

SIZE   N/A
DATE: Monday, September 21, 2015
SCALE = NONE

REV. 1
SHEET 1 OF 2

SCHEMATIC DIAGRAM

Note: The buffers shown on sheet 2 of 2 of the schematic are used to protect the LTC6948 when connected to the DC590 before the LTC6948 is powered up. There is no need for such circuitry if the SPI bus is not active before powering up the LTC6948. The EEPROM is for identification and is not needed to program the LTC6948.

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