TS4100/01/02 Data Sheet

"Rail-to-Rail Plus"™, 1% RON Flatness, 0.8 V to 5.25 V Analog Switches/Multiplexers

The TS410x family of analog switches and multiplexers consists of the TS4100 8-channel analog multiplexer, the TS4101 dual 4-channel analog multiplexer, and the TS4102 triple single-pole/double-throw (SPDT) switch. These switches are unique because they can operate at supply voltages as low as 0.8 V while accepting input signal swings above the supply voltage up to 5.25 V ("Rail-to-Rail Plus"™). The on-resistance variation over the entire signal swing range is less than 1%, exhibiting excellent linearity and consistency in dynamic and measurement applications. With a supply current of only 675 nA, the TS4100-TS4102 family input and output leakage is less than 0.5 nA, both when off and when on.

The TS4100-TS4102 are fully specified over the –40 °C to +85 °C temperature range and is available in a low-profile, thermally-enhanced 16-pin 3.3 mm TQFN package with an exposed back-side paddle. For best performance, solder exposed back-side paddle to PCB ground.

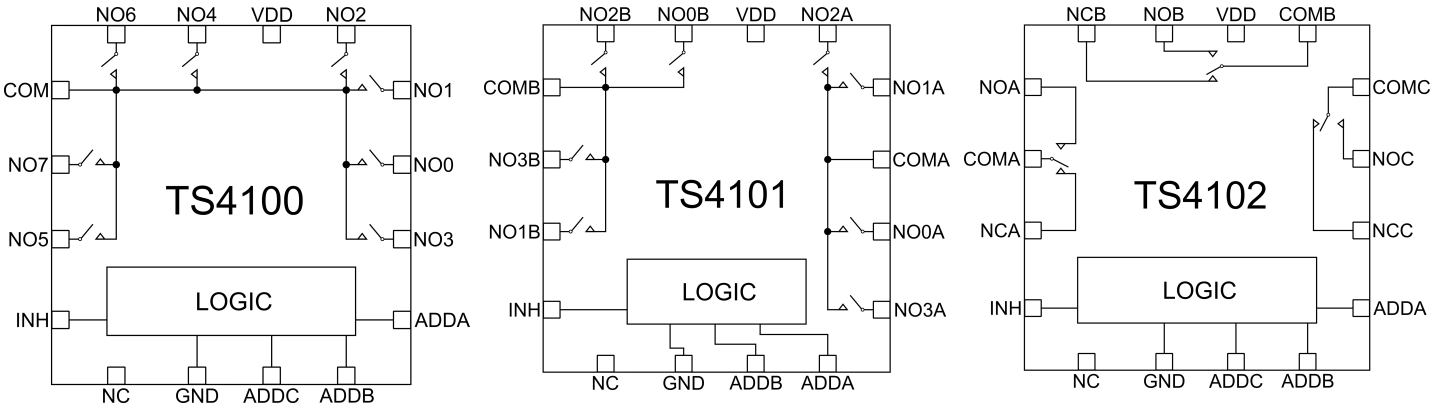
Applications

- Low Voltage Battery-Operated Equipment
- Precision Measurement
- Analog Signal Processing
- Communication Circuits
- Audio Signal Routing
- Low-Voltage Data-Acquisition Systems

KEY FEATURES

- Low Supply Voltage Operation: 0.8 V to 5.25 V
- On-resistance of 80 Ω
- "Rail to Rail Plus"™ input/output voltages can exceed the supply rails
- Guaranteed Low Off and On Leakage: ±0.5 nA
- Guaranteed Match Between Channels: 9 Ω
- Guaranteed <1% On-Resistance Variation Across Input Voltage
- TS4100: 8-Channel Switch/Multiplexer
- TS4101: Two 4-Channel Switches/ Multiplexers
- TS4102: Three Single-Pole/Double-Throw Switches (SPDT)
- Supply Current: 675 nA
- 16-Pin, Low-Profile, Thermally Enhanced 3 mm x 3 mm TQFN Package

Functional Block Diagrams



1. Ordering Information

Ordering Part Number	Description	Package
TS4100ITQ1633	8:1 analog multiplexer	TQFN-16 (3 x 3 mm)
TS4101ITQ1633	Two 4:1 analog multiplexers	TQFN-16 (3 x 3 mm)
TS4102ITQ1633	Three 2:1 SPDT analog switches	TQFN-16 (3 x 3 mm)

Note:

1. Adding the suffix “T” to the part number (e.g., TS4100ITQ1633T) denotes tape and reel.

2. System Overview

The TS4100 is an 8-channel multiplexer with inputs NO0-NO7 and output COM. A channel can be selected via address pins ADDA, ADDB, and ADDC.

The TS4101 is a dual 4-channel switch/multiplexer with two separate input banks: NO0A-NO3A and NO0B-NO3B with dedicated output COMA and COMB, respectively. A channel can be selected via address pins ADDA and ADDB.

The TS4102 is a triple single-pole/double-throw (SPDT) switch. When ADDA, ADDB, or ADDC is set to a Low state, the output will be NCA, NCB, or NCC, respectively. When ADDA, ADDB, or ADDC is set to a High state, the output will be NOA, NOB, or NOC, respectively. Refer to XREF DIGITAL I/O SETTINGS TABLE

Unlike similar switch/multiplexer devices, the TS4100-TS4102 input voltage is independent of the supply voltage. This allows the input voltage to be greater than the supply voltage while maintaining a flat On-resistance vs. the VNO/VCOM curve. Refer to 3.1 Typical Performance Characteristics for more information.

2.1 Applications Information

2.1.1 AC Performance Considerations

2.1.2 Off Isolation

Like all switch/multiplexer devices, the off-isolation of the device is measured when the device is off (see Figure 2.8 TS4100-TS4102 Charge Injection Test Setup on page 8). During the OFF state, part of the input signal couples to the output load. To maximize the off-isolation, maximize your capacitive load and minimize your resistive load. The trade-off is that this can increase the insertion loss of the device so it must be considered when designing a circuit. The insertion loss is measured when the switch/multiplexer is in the ON state (see Figure 2.9 TS4100-TS4102 Off-Isolation Test Setup on page 9).

At 10 kHz, the off-isolation of the TS4100-TS4102 is approximately –88 dB. Refer to the Off-Isolation vs. Frequency plot in 3.1 Typical Performance Characteristics.

2.1.3 Total Harmonic Distortion (THD)

In audio and data acquisition applications, signal fidelity is of a concern. As a result, the THD parameter of the analog mux/switch becomes an important factor. Many current analog switch/mux devices on the market implement a design that allow for a large variation of on-resistance as the input signal is changing. With 1% on-resistance variation over the entire signal swing, the TS4100-TS4102 design minimizes THD. At 10 kHz, the TS4100-TS4102 exhibits a THD of 0.15% over the entire signal swing.

2.1.4 Bandwidth Considerations

The magnitude of the output resistive load and capacitive load has an impact on the bandwidth of the mux/switch. At dc or close to dc input signals, a resistive load has the greatest impact where the output voltage is determined primarily by the voltage divider consisting of the switch on-resistance and the output resistive load. To minimize the ON insertion loss, maximize the resistive load.

As the input frequency increases, the ac impedance of the circuit begins to have an impact on bandwidth of the mux/switch. To counter this effect, minimize the load capacitance and any stray capacitance that may be present on the board. Also, ensure a board layout that minimizes signal trace lengths.

2.1.5 Programmable Gain Amplifier (PGA) with the TS4100

Analog signals can vary in amplitude and frequency especially when considering various taypes of sensors such as thermistors, strain gauges, and photodiodes. To process the analog signals provided by the sensor, a stand-alone ADC such as a TS7001 or TS7003 can be used. However, to take advantage of the resolution of the ADC, the analog signals must be scaled up to the maximum input voltage range of the ADC.

One way to achieve this is by designing a 1.5 V non-inverting programmable gain amplifier (PGA) that incorporates a TS1005 operational amplifier and a TS4100 analog multiplexer as shown in the figure below. The gain can be changed from 2 to 8 via address pins ADDA, ADDB, and ADDC.

With the TS4100 connected to ground, the on-resistance of the switch becomes part of the gain of the amplifier and needs to be accounted for in the following gain equation: $GAIN = 1 + \frac{R1}{RGX + RON}$

where RON is 80 Ω (typ) and RGX is the resistor connected to the TS4100 input. Unlike other analog switches, the TS4100 on-resistance variation over the entire signal swing range is less than 1%. In this circuit, the corresponding gain variation is less than 0.03% across all channels. This circuit accommodates an input signal bandwidth of 2.5 kHz to 10 kHz. Also, by connecting the TS4100 to ground, internal switching spikes are minimized. Refer to 2.1.7 Charge Pump Effect Considerations.

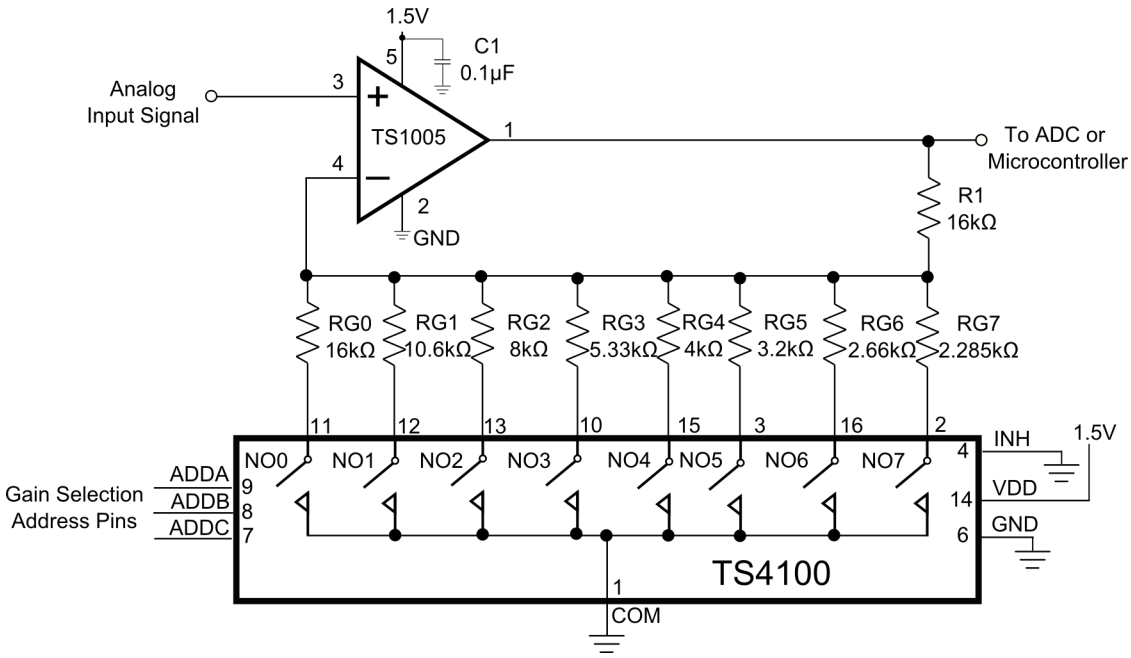


Figure 2.1. Non-Inverting Programmable Gain Amplifier (PGA) with TS4100

2.1.6 Switched-Capacitor Voltage Doubler with the TS4102 and TS3004 Timer

In portable applications, it is a common requirement for a battery to continue to supply power to a circuit when it has discharged to a voltage unusable by other devices in the system. To address this, a simple voltage doubler can be designed using two SPDT switches in a single TS4102 device and a TS3004 timer as shown in the figure below.

In this configuration, the TS3003 timer FOUT output provides a 200 Hz (50% Duty Cycle) clock signal to address pin ADDA and ADDB that switches between 0 V and VDD. When the clock signal to the address pins ADDA and ADDB is 0 V, capacitor C1 is charged to VSUPPLY. When the clock input is VDD, the charge in C1 is passed to C2 and effectively doubles the voltage at NOB to 2 x VSUPPLY.

Unlike other analog switches, the TS4102 allows the supply voltage to be independent of the common mode input voltage. In this configuration, the TS4102 allows the supply voltage to be independent of the common mode input voltage. In this configuration, the TS4102 and the TS3004 can operate at a supply voltage range of 1.55 V to 5.25 V while the output voltage is 5 V with VSUPPLY = 2.5 V. With VDD = 1.55 V, the complete circuit consumes only 3 µA of supply current and can drive an output load of up to 48 µA (5% drop at VOUT).

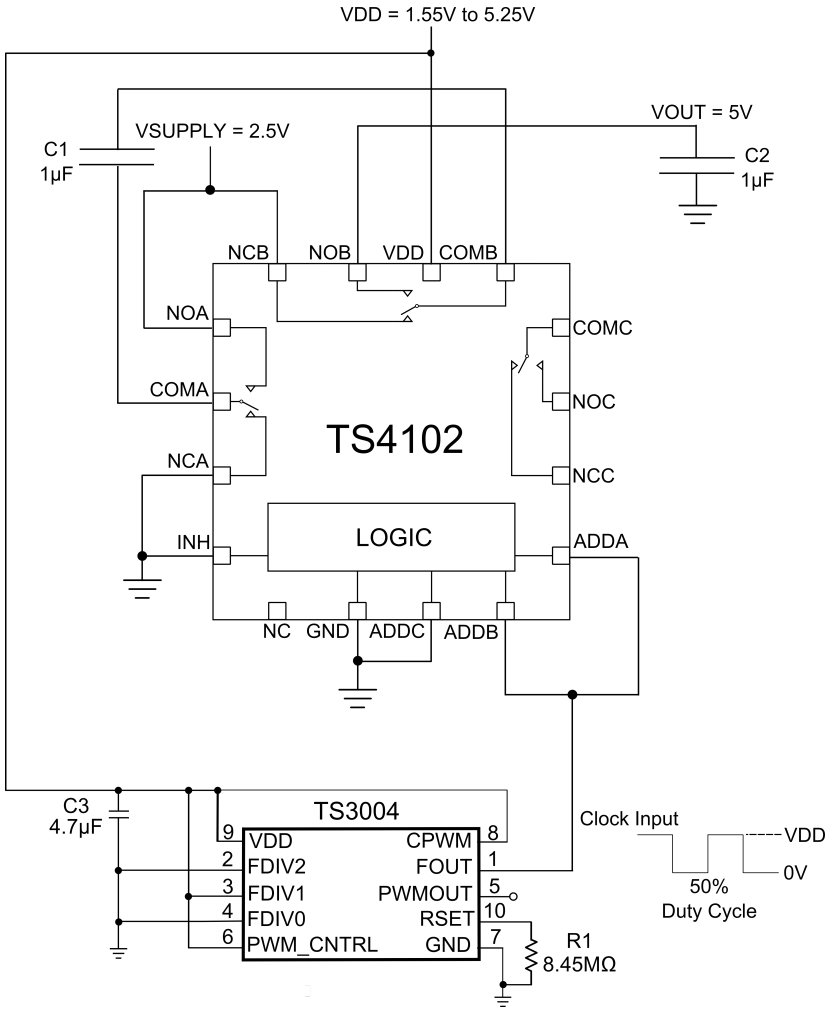


Figure 2.2. Switched-Capacitor Voltage Doubler with TS4102 and TS3004 Timer

2.1.7 Charge Pump Effect Considerations

The on-resistance of a MOSFET is inversely proportional to the overdrive voltage in the region where MOSFETS are used as switches. Conventional analog switch/multiplexers derive their overdrive voltage directly from the supply voltage and common mode input voltage; hence, the on-resistance varies with the supply voltage or common mode input voltage.

The TS4100-TS4102 maintains a flat on-resistance that is independent of the supply voltage or common mode input voltage. To achieve this, a charge pump scheme is implemented where a constant overdrive voltage is applied across the MOSFET. The charge pump is refreshed at a period of 40 µs with a time period variation of up to 2X.

In applications where input and output impedance is high in the order of MΩs, transients generated by the charge pump can couple to the input and output of the device. The pulse width of the spikes is 10-s of nanoseconds. The amplitudes of the spikes are independent of the operating conditions, such as temperature, common mode input voltage and supply voltage.

The figures below show a scope capture of these spikes with an input/output impedance of 1 MΩ and 10 MΩ. With an input/output impedance of 1 MΩ and 10 MΩ, the amplitude of the spikes is less than 200 µV and 500 µV, respectively.

If these spikes are of a concern in the application, placing a 500 pF capacitor to ground at the input or output will suppress the spikes.

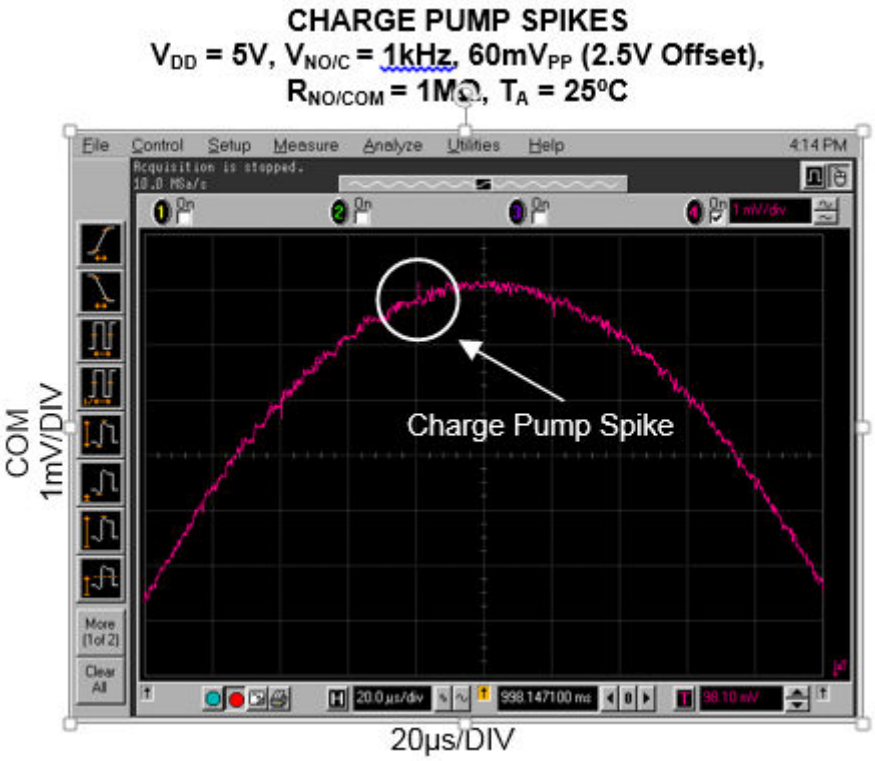


Figure 2.3. Charge Pump Spike ($R_{NO/COM}$ = 1 MΩ)

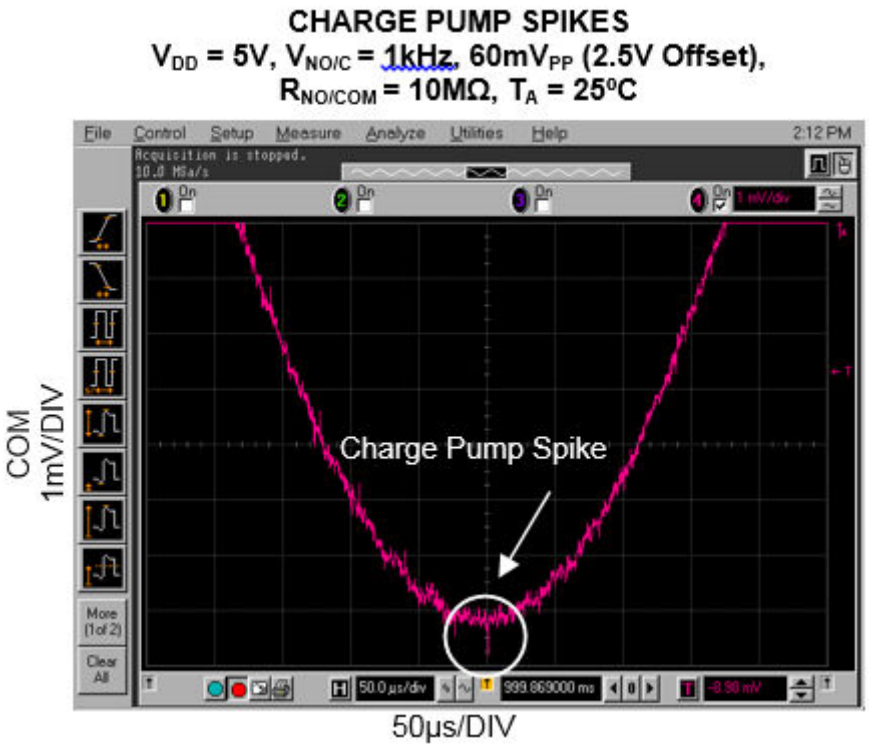


Figure 2.4. Charge Pump Spike ($R_{NO/COM}$ = 10 MΩ)

2.1.8 Power-Up Sequence

To prevent permanent damage to the ADDA, ADDB, ADDC, and INH pin, the power supply voltage should be applied to the device first followed by the voltage to ADDA, ADDB, ADDC, and/or INH. If it is not possible to follow this power-supply sequence, a 500kΩ resistor can be placed in series with the digital I/O pins for protection as shown in the figure below. However, if an input voltage is applied before applying power to the switch/multiplexer, the device will not be damaged as the inputs are independent of the supply voltage.

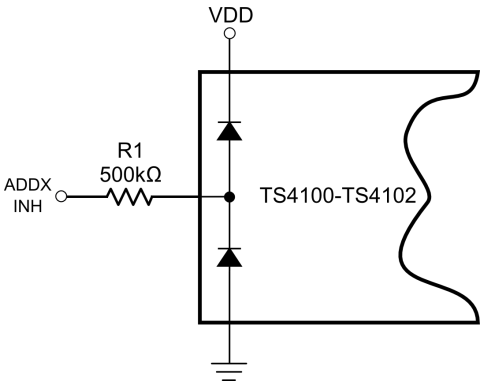


Figure 2.5. Digital I/O Overvoltage Protection

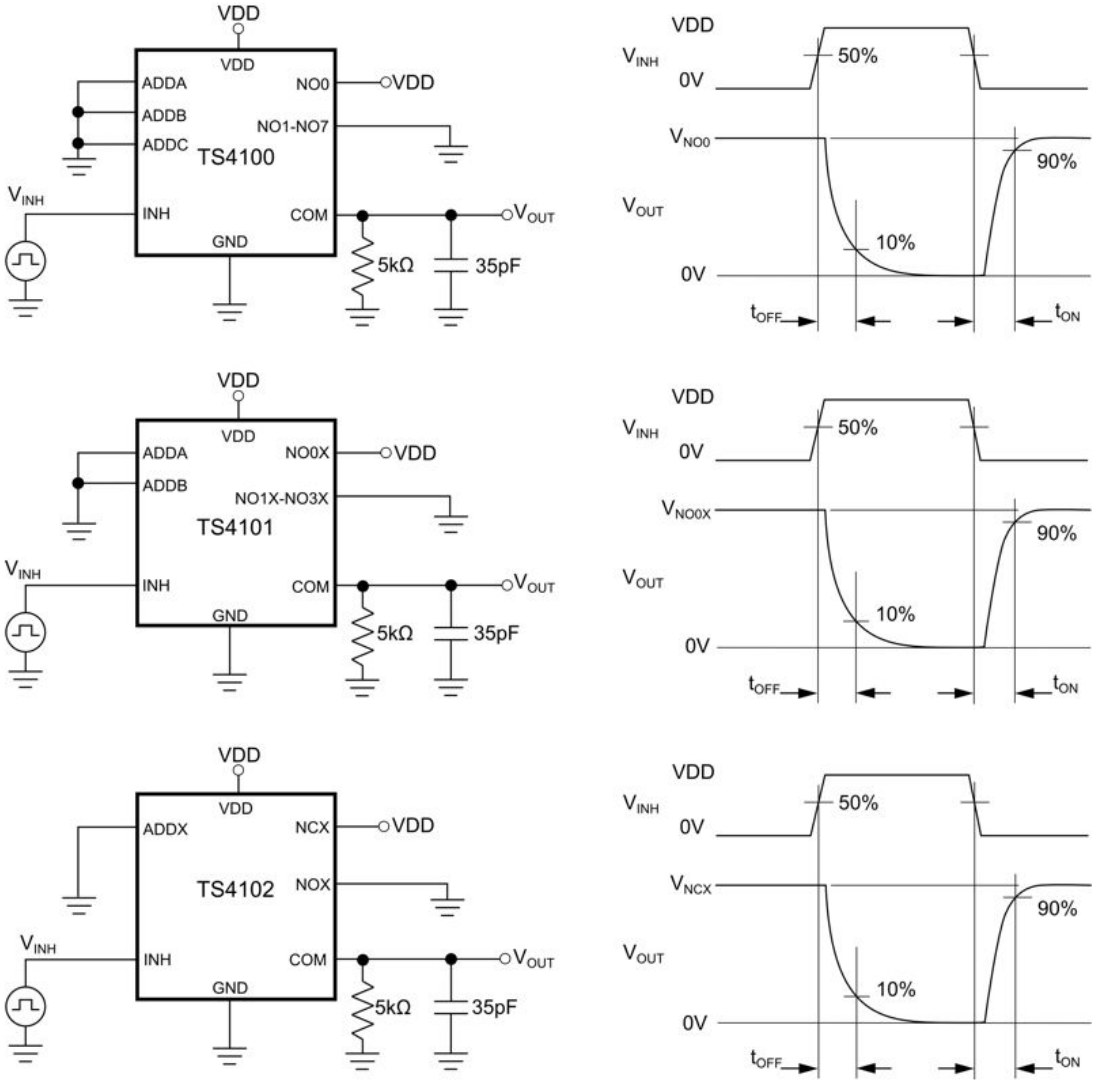


Figure 2.6. TS4100-TS4102 Address/Enable Turn-On/Off Time Test Setup

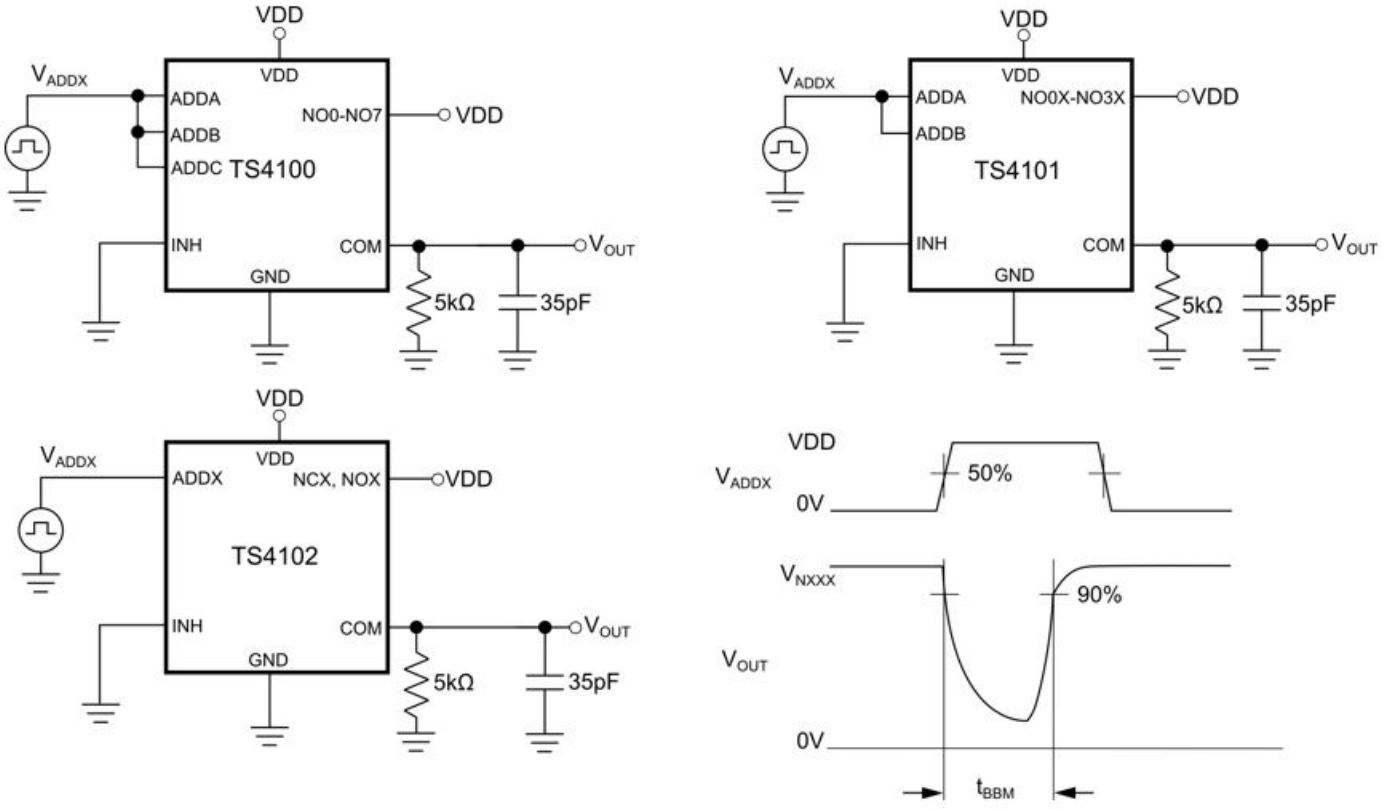


Figure 2.7. TS4100-TS4102 Break-Before-Make Test Setup

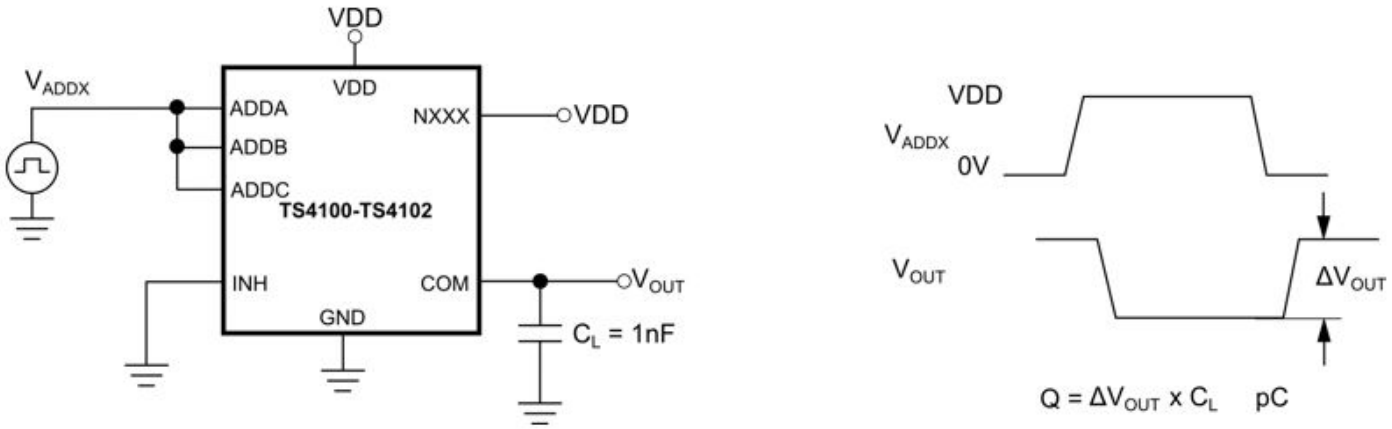


Figure 2.8. TS4100-TS4102 Charge Injection Test Setup

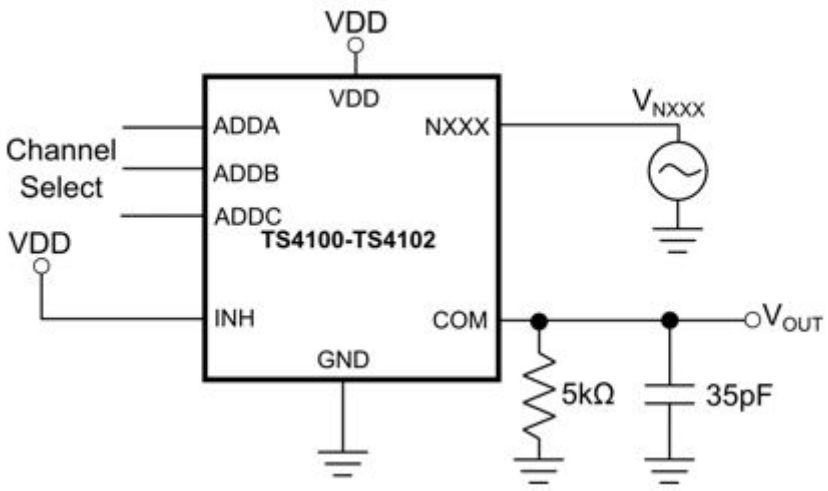


Figure 2.9. TS4100-TS4102 Off-Isolation Test Setup

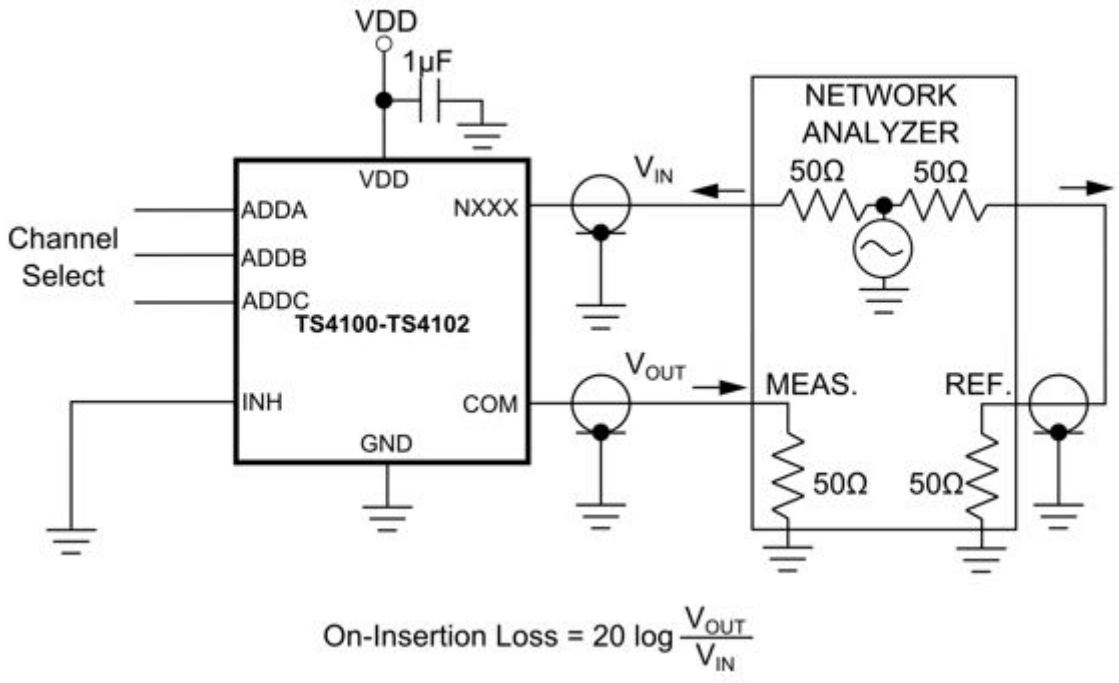


Figure 2.10. TS4100-TS4102 Insertion Loss Test Setup

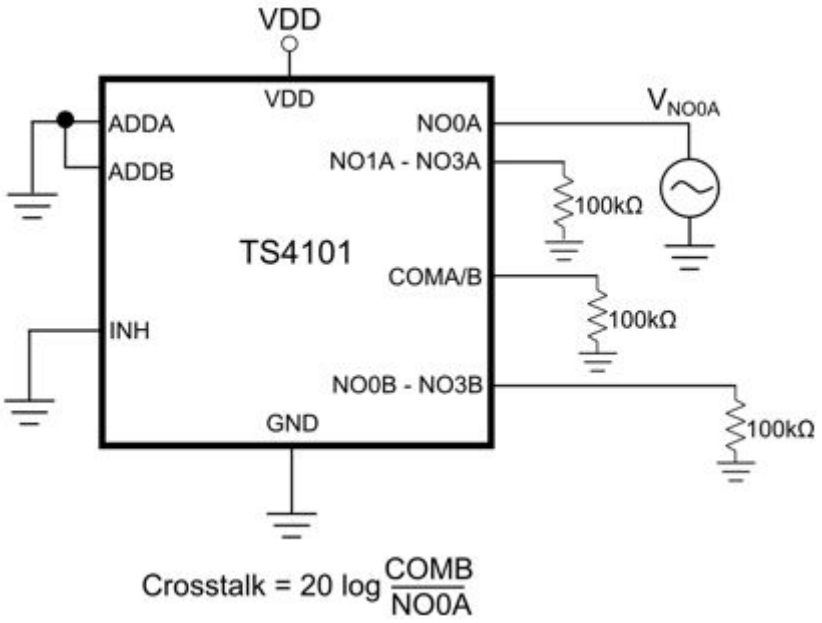


Figure 2.11. TS4101 Crosstalk Test Setup

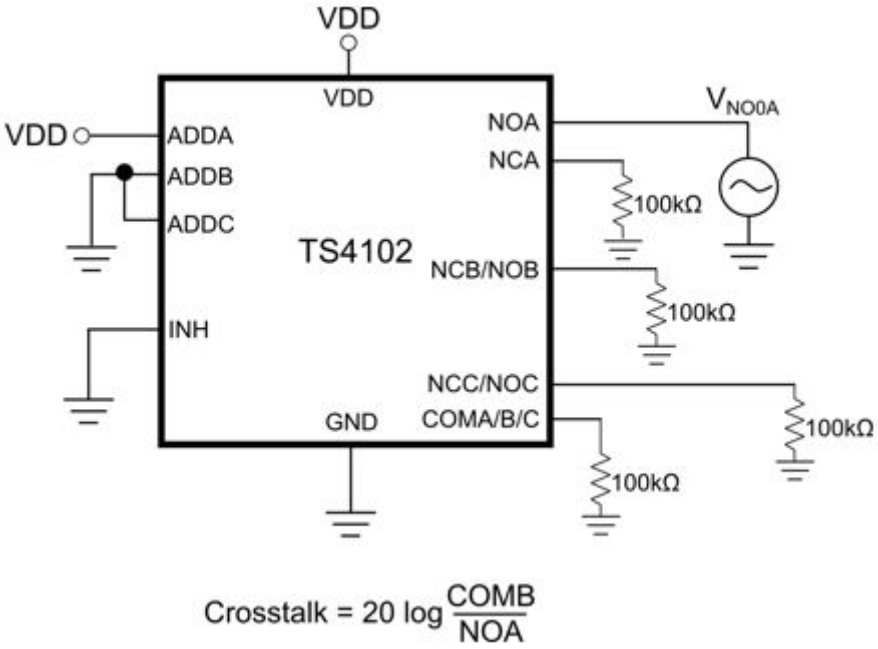


Figure 2.12. TS4102 Crosstalk Test Setup

3. Electrical Characteristics

Table 3.1. Recommended Operating Conditions[1]

Parameter	Symbol	Conditions		Min	Typ	Max	Units
Analog Switch							
Analog Signal Range	$V_{NO/C}$, V_{COM}			0		5.25	V
On Resistance	R_{ON}	0.8 V ≤ V_{DD} < 1.25 V I_{COM} = 1 mA	T_A = 25 °C		98	105	Ω
						135	Ω
		1.25 V ≤ V_{DD} ≤ 5.25 V I_{COM} = 1 mA	T_A = 25 °C		80	90	Ω
						130	Ω
On Resistance Flatness	RON_{FLAT}	0 V ≤ $V_{NO/C}$ ≤ 5.25 V I_{COM} = 1 mA[2,3]	T_A = 25 °C			1	%
						1.5	%
On-Resistance Match Between channels	ΔR_{ON}	V_{DD} = 5 V $V_{NO/C}$ = 5 V I_{COM} = 1 mA[4]			2.25	9	Ω
NO/NC Off-Leakage Current	$I_{NO/NC(OFF)}$	VDD = 5.25 V	T_A = 25 °C	–0.5		0.5	nA
		$V_{NO/C}$ = 0 V or 5.25 V V_{COM} = 0 V or 5.25 V INH = 5.25 V[5]		–2		2	nA
TS4100-TS4102 COM Off-Leakage Current	$I_{COM(OFF)}$	V_{DD} = 5.25 V	T_A = 25 °C	–0.5		0.5	nA
		$V_{NO/C}$ = 0 V or 5.25 V V_{COM} = 0 V or 5.25 V INH = 5.25 V[5]		–2		2	nA
COM On-Leakage Current	$I_{COM(ON)}$	V_{DD} = 5.25 V, $V_{NO/C}$ = V_{COM} = 5.25 V[5]	T_A = 25 °C	–0.5		0.5	nA
				–4		4	nA
Digital I/O							
ADDA/B/C, INH Input Logic High	V_{IH}			0.6			V
ADDA/B/C, INH Input Logic Low	V_{IL}					0.2	V
ADDA/B/C, INH Input Leakage Current	I_{IH}, I_{IL}	V_{INH} = $V_{ADDA/B/C}$ = 0 or 5.25 V		–2		2	nA
Switch Dynamic Characteristics							

Parameter	Symbol	Conditions		Min	Typ	Max	Units
ADDA/B/C, INH Turn-On Time	t_{ON}	V_{DD} = 5.25 V R_L = 5 kΩ, C_L = 35 pF See Figure 2.6 TS4100-TS4102 Address/Enable Turn-On/Off Time Test Set-up on page 7			7	9	µs
ADDA/B/C, INH Turn-Off Time	t_{OFF}				0.5	0.8	µs
Break-Before-Make Delay	t_{BBM}	$V_{NO/C}$ = 5.25 V R_L = 5 kΩ, C_L = 35 pF See Figure 2.7 TS4100-TS4102 Break-Before-Make Test Setup on page 8[6]			6.5	8.2	µs
Charge-Injection	Q	$V_{NO/C}$ = 5.25 V, C_L = 1 nF See Figure 2.8 TS4100-TS4102 Charge Injection Test Setup on page 8.			10		pC
Off-Isolation	V_{ISO}	f = 10 kHz, $V_{NO/C}$ = 1 V_{RMS}, R_L = 100 kΩ, C_L = 50 pF See Figure 2.9 TS4100-TS4102 Off-Isolation Test Setup on page 9.			–87		dB
TS4101,TS4102 Crosstalk	V_{CT}	f = 10 kHz, $V_{NO/C}$ = 1 V_{RMS}, R_L = 100 kΩ See Figure 2.11 TS4101 Crosstalk Test Setup on page 10 and Figure 2.12 TS4102 Crosstalk Test Setup on page 10.			–77		dB
Total Harmonic Distortion	THD	f = 10 kHz, $V_{NO/C}$ = 400 mV_{PP} (500 mV Offset) C_L = 15 pF, $R_{NO/C}$ = R_{COM} = 600 Ω			0.16		%
Power Supply							
Supply Current	I_Q	V_{DD} = 5.25 V	T_A = 25 ºC		675	765	nA
		$V_{NO/C}$ = 0 or V_{DD}				950	nA
Supply Voltage	V_{DD}			0.8		5.25	V

Note:

1. V_{DD} = 0.8 V to 5.25 V; INH = GND unless otherwise specified; T_A= –40 °C to +85 °C. Typical values are at T_A = +25 °C; All specifications are 100% tested at T_A = +85°C. Specification limits over temperature (T_A = T_{MIN} to T_{MAX}) are guaranteed by device characterization, not production tested.
2. On-Resistance Flatness is defined by the following equation: ($RON_{0.5V}$ – $RON_{5.25V}$ / $RON_{0.5V}$) x 100.
3. Tested at $V_{NO/C}$ = 0.5 V and $V_{NO/C}$ = 5.25 V and guaranteed by design from $V_{NO/C}$ = 0 V to $V_{NO/C}$ = 5.25 V.
4. $\Delta RON = RON_{MAX} - RON_{MIN}$
5. Leakage parameters are guaranteed by correlation at T_A = 25 ºC and are 100% tested at the maximum rated hot operating temperature.
6. t_{BBM} = t_{ON} − t_{OFF}. Not production tested.

Table 3.2. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Units
Supply Voltage	V_{DD}		–0.3	+5.5	V
Analog Signal Voltage	$V_{NO/C}$, V_{COM}		–0.3	+5.5	V
Digital Signal Voltage	$V_{ADDA/B/C}$, V_{INH}		–0.3	VDD + 0.3	
Analog Peak Current	$I_{NO/C}$, I_{COM}			±15	mA
Continuous Power Dissipation	P_D	T_A = +70 °C[2]		1398	mW
Operating Temperature			–40	+85	°C
Storage Temperature			–65	+150	°C
Lead Temperature (Soldering, 10 s)				+300	°C
ESD Tolerance					
Human Body Model				1000	V
Machine Model				200	V

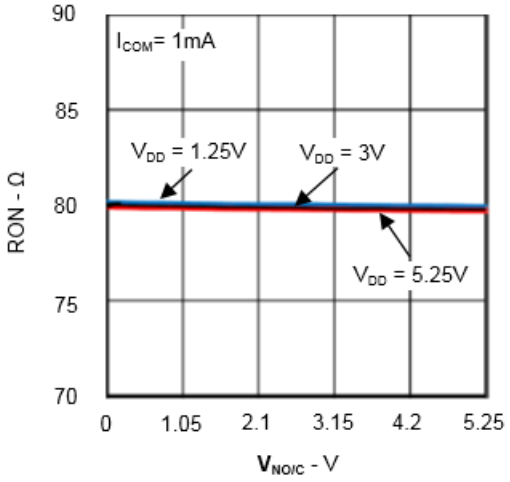
Note:

1. Electrical and thermal stresses beyond those listed in this table may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to any absolute maximum rating conditions for extended periods may affect device reliability and lifetime.
2. Derate at 17.5 mW/°C above +70 °C.

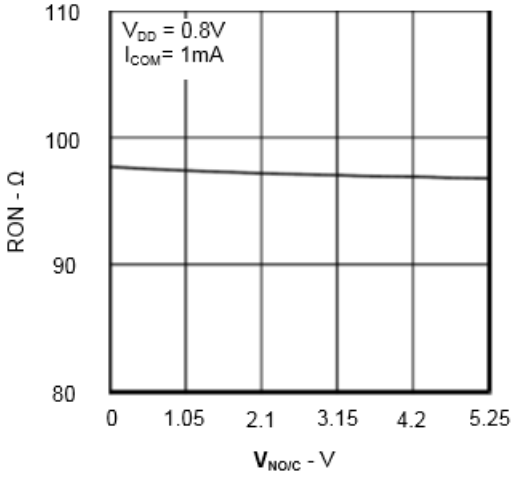
3.1 Typical Performance Characteristics

For the following graphs, VDD = 5.25 V, CL = 0 pF, RL = No load, INH = Low, unless otherwise noted. Values are at TA = 25 °C unless otherwise noted.

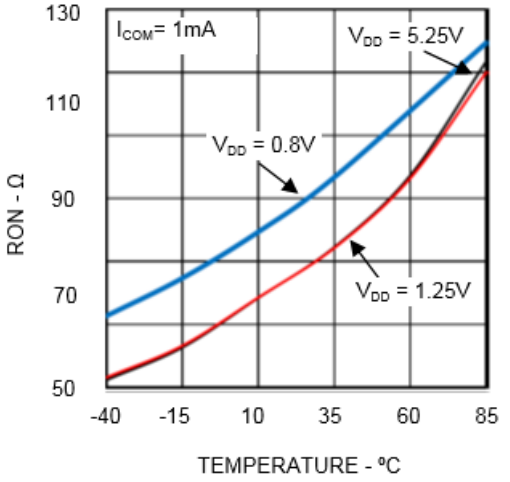
On-Resistance vs $V_{NO/C}$



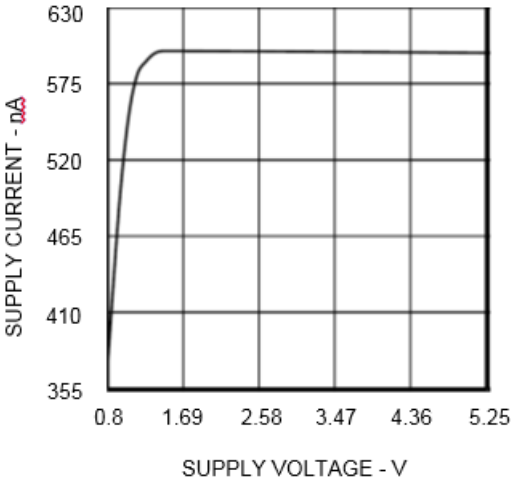
On-Resistance vs $V_{NO/C}$



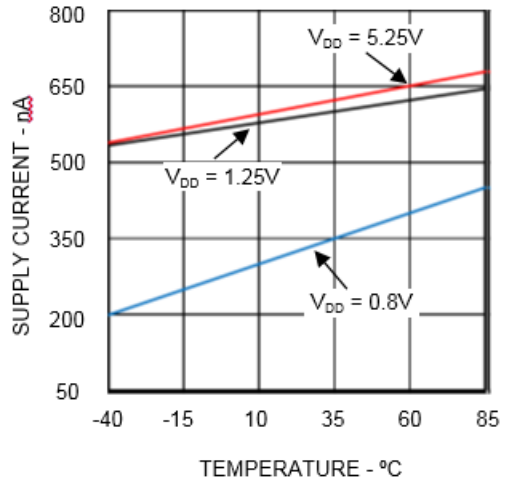
RON vs Temperature



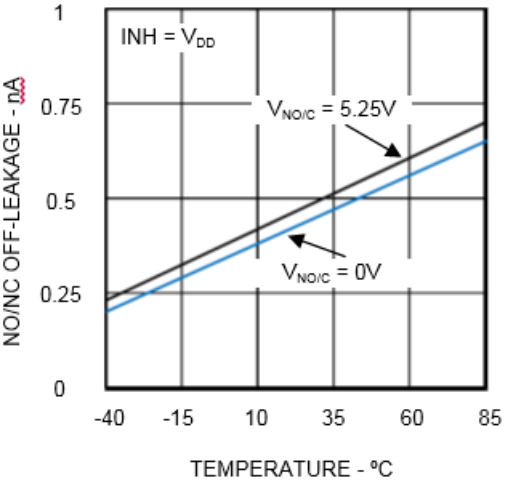
Supply Current vs Supply Voltage



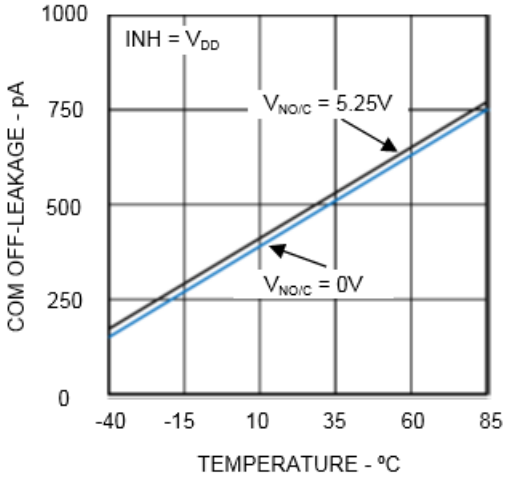
Supply Current vs Temperature



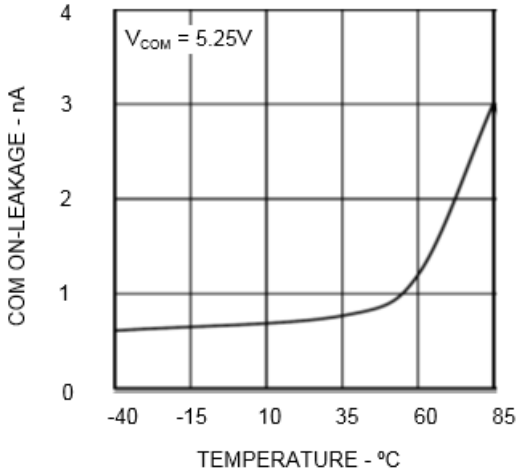
NO/NC Off-Leakage vs Temperature



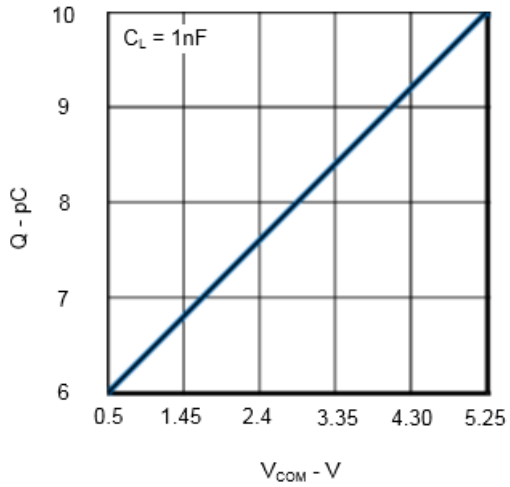
COM Off-Leakage vs Temperature



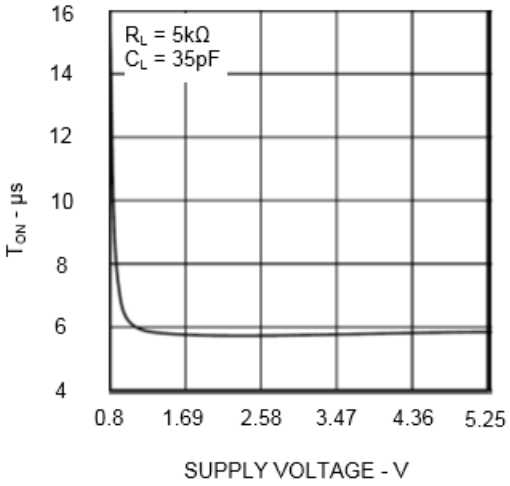
COM On-Leakage vs Temperature



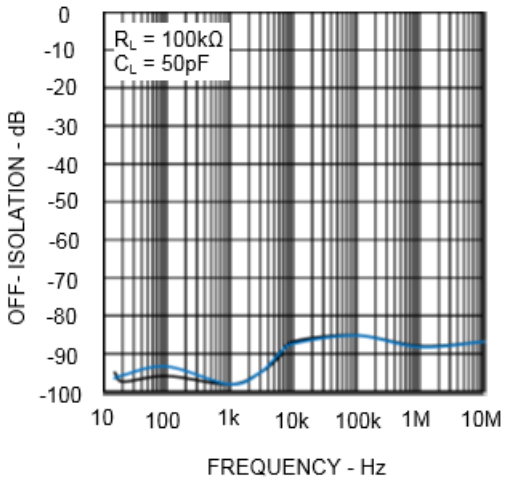
Charge Injection vs V_{COM}



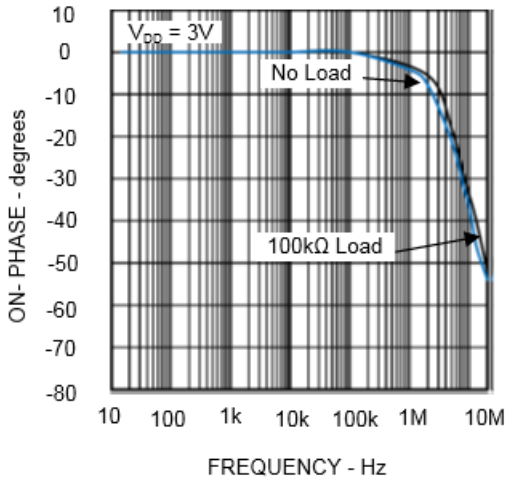
T_{ON} Time vs Supply Voltage



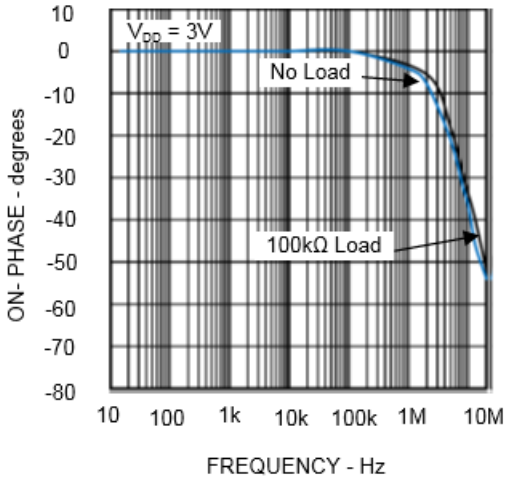
Off-Isolation vs Frequency



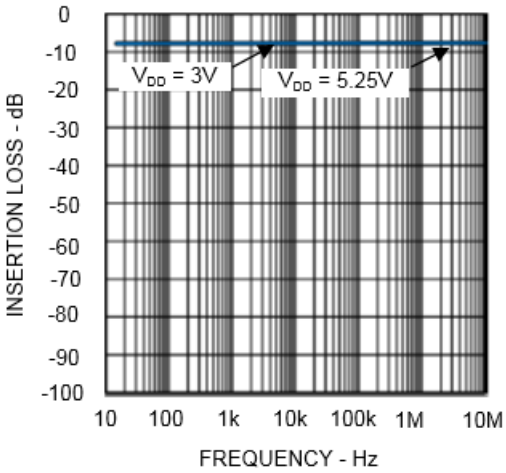
On-Phase vs Frequency



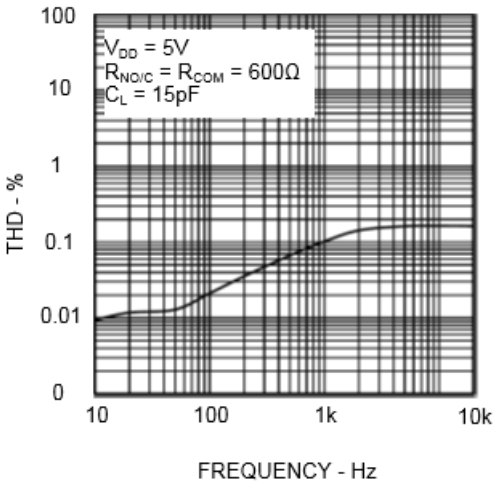
On-Phase vs Frequency



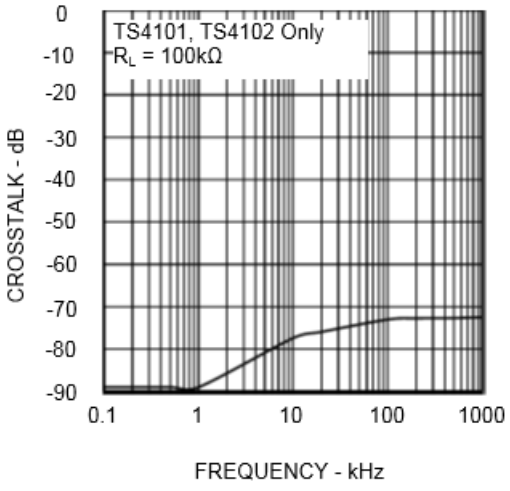
Insertion Loss vs Frequency



Total Harmonic Distortion vs Frequency



Crosstalk vs Frequency



4. Pin Descriptions

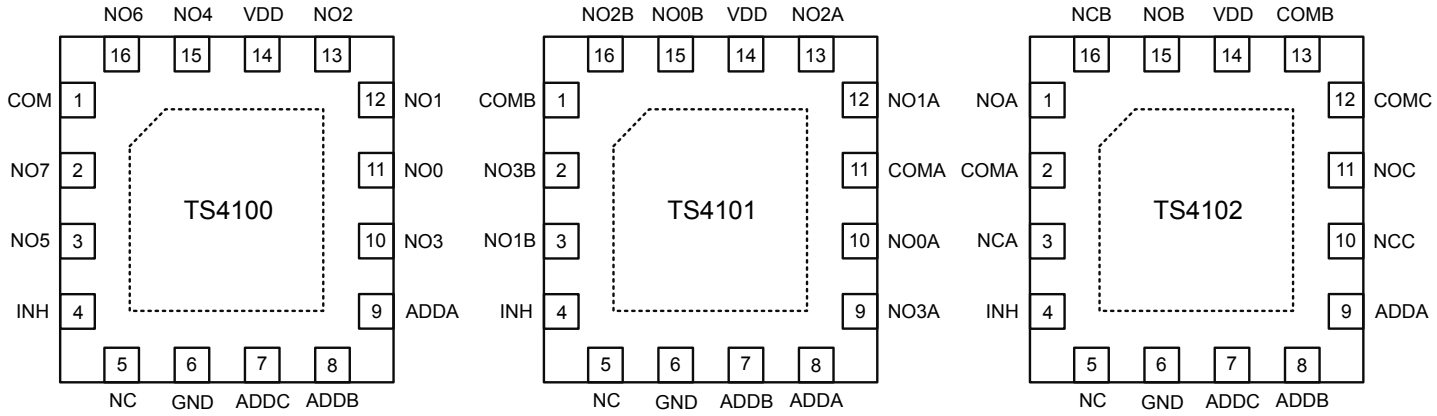


Table 4.1. Pin Functions

Pin	Pin Name			Function
	TS4100	TS4101	TS4102	
1	COM			8-channel switch/multiplexer output
		COMB		4-channel switch/multiplexer "B" output
			NOA	Single-Pole/Double-Throw Switch (SPDT) "A" normally open input.
2	NO7			8-channel switch/multiplexer input.
		NO3B		4-channel switch/multiplexer "B" input.
			COMA	Single-Pole/Double-Throw Switch (SPDT) "A" output.
3	NO5			8-channel switch/multiplexer input
		NO1B		4-channel switch/multiplexer "B" input.
			NCA	Single-Pole/Double-Throw Switch (SPDT) "A" normally closed input.
4	INH			Enable digital I/O input. To enable the switch/multiplexer, connect to GND. To disable, connect to VDD. Refer to the "Digital I/O Overvoltage Protection" section of the data sheet.
5	NC			No Connect.
6	GND			Ground. Connect this pin to the system's clean analog ground plane.
7	ADDC		ADDC	Address "C" digital I/O input. Refer to the "Digital I/O Overvoltage Protection" section of the datasheet.
		ADDB		Address "B" digital I/O input. Refer to the "Digital I/O Overvoltage Protection" section of the datasheet.
8	ADDB		ADDB	
		ADDA		Address "A" digital I/O input. Refer to the "Digital I/O Overvoltage Protection" section of the datasheet.
9	ADDA		ADDA	
		NO3A		4-channel switch/multiplexer "A" input.
10	NO3			8-channel switch/multiplexer input.
		NO0A		4-channel switch/multiplexer "A" input.
			NCC	Single-Pole/Double-Throw Switch (SPDT) "C" normally closed input.

Pin	Pin Name			Function
	TS4100	TS4101	TS4102	
11	NO0			8-channel switch/multiplexer input.
		COMA		4-channel switch/multiplexer "A" output.
			NOC	Single-Pole/Double-Throw Switch (SPDT) "C" normally open input.
12	NO1			8-channel switch/multiplexer input.
		NO1A		4-channel switch/multiplexer "A" input
			COMC	Single-Pole/Double-Throw Switch (SPDT) "C" output.
13	NO2			8-channel switch/multiplexer input.
		NO2A		4-channel switch/multiplexer "A" input.
			COMB	Single-Pole/Double-Throw Switch (SPDT) "B" output.
14	VDD			Power Supply Voltage Input. Bypass this pin with a 1µF cerarnic coupling capacitor in close proximity to the TS4100-TS4102.
15	NO4			8-channel switch/multiplexer input.
		NO0B		4-channel switch/multiplexer "B' input.
			NOB	Single-Pole/Double-Throw Switch (SPDT) "B" normally open input.
16	NO6			8-channel switch/multiplexer input
		NO2B		4-channel switch/multiplexer "B" input.
			NCB	Single-Pole/Double-Throw Switch (SPDT) "B" normally closed input.
EP	—	—	—	For best electrical and thermal performance, solder exposed paddle to GND.

4.1 Digital I/O Settings

Table 4.2. Digital I/O Settings

INH	Address Bits			TS4100	TS4101		TS4102		
	ADDC (TS4100 and TS4102 Only)	ADDB	ADDA	COM Output	COMA Output	COMB Output	COMA Output	COMB Output	COMC Output
1	**X**	**X**	**X**	**Switch Open**					
0	0	0	0	NO0	NO0A	NO0B	NCA	NCB	NCC
0	0	0	1	NO1	NO1A	NO1B	NOA	NCB	NCC
0	0	1	0	NO2	NO2A	NO2B	NCA	NOB	NCC
0	0	1	1	NO3	NO3A	NO3B	NOA	NOB	NCC
0	1	0	0	NO4	NO0A	NO0B	NCA	NCB	NOC
0	1	0	1	NO5	NO1A	NO1B	NOA	NCB	NOC
0	1	1	0	NO6	NO2A	NO2B	NCA	NOB	NOC
0	1	1	1	NO7	NO3A	NO3B	NOA	NOB	NOC

5. Packaging

5.1 TS410x Package Dimensions

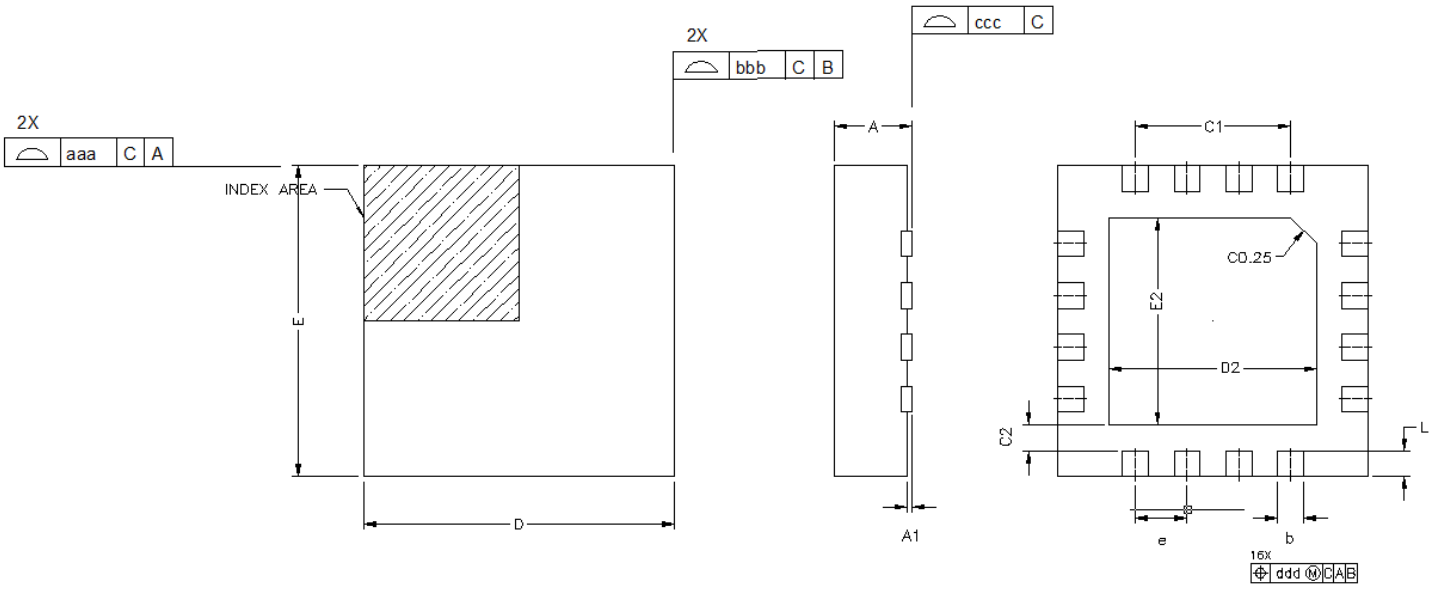


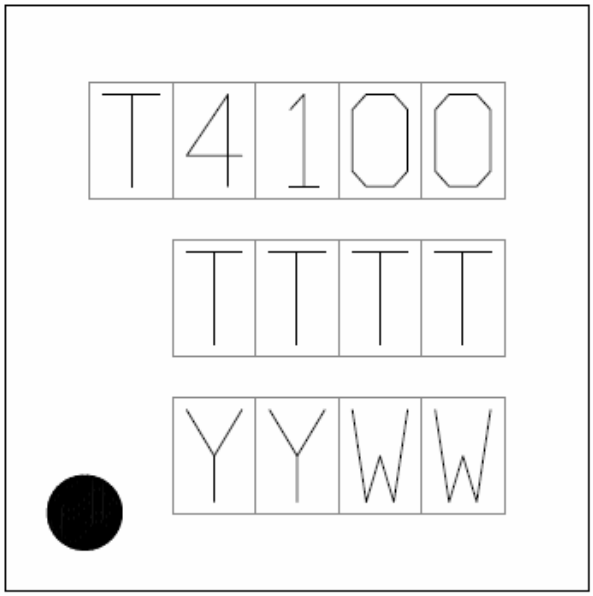
Figure 5.1. 3x3 mm 16-QFN Package Diagram

Dimension	Min	Nom	Max
A	0.70	0.75	0.85
A1	0.00	—	0.05
b	0.20	0.25	0.30
D		3.00 BSC.	
D2	1.75	1.80	1.85
e		0.50 BSC.	
E		3.00 BSC.	
E2	1.75	1.80	1.85
L	0.30	0.35	0.40
aaa	—	—	0.05
bbb	—	—	0.05
ccc	—	—	0.05
ddd	—	—	0.10

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

5.2 TS410x Top Marking



TS4100 Top Marking

Table 5.1. TS4100 Top Marking Explanation

Mark Method:	Laser	
Pin 1 Mark:	Circle = 0.5 mm Diameter (Lower-Left Corner)	
Font Size:	0.50 mm (20 mils)	
Line 1 Mark Format:	Product ID	e.g., "T4100"
Line 2 Mark Format:	TTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order Form.
Line 3 Mark Format:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the assembly release.

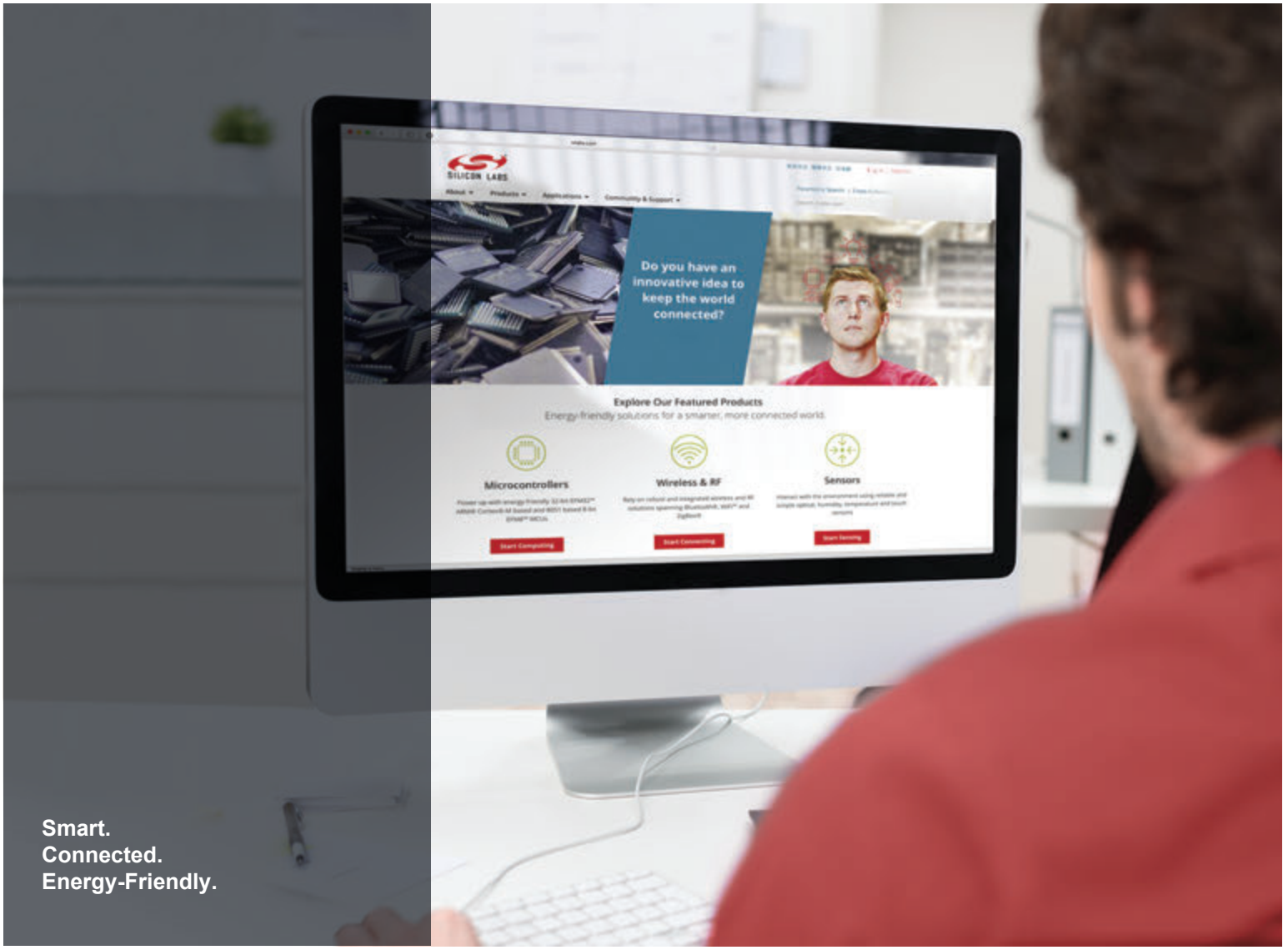
6. Revision History

Revision 1.0

February 24, 2016

- Initial external release.

Table of Contents



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