SPC564A74xx, SPC564A80xx Errata sheet

SPC564A74xx, SPC564A80xx device errata JTAG_ID = 0x1AE02041

Introduction

This errata sheet describes all the functional and electrical problems known in the revision 2.0 of the SPC564A74xx, SPC564A80xx, devices, identified with the JTAG_ID = 0x1AE02041.

All the topics covered in this document refer to *RM0029* rev 7 and *SPC564A74B4, SPC564A74L7, SPC564A80B4, SPC564A80L7 datasheet* rev 8 (see *Section A.1: Reference document*).

Device identification:

- Package device marking mask identifier: BAG
- JTAG_ID = 0x1AE02041
- MIDR register:
  - MAJOR_MASK[3:0]: 1
  - MINOR_MASK[3:0]: 0

This errata sheet applies to SPC564A74xx, SPC564A80xx, devices in accordance with *Table 1*.

Table 1. Device summary

Part number	Package
SPC564A74L7	LQFP176
SPC564A74B4	PBGA324
SPC564A80L7	LQFP176
SPC564A80B4	PBGA324

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1 Functional problems

1.1 ERR003285: SIU: MCU ID register package information not reliable on the calibration package

Description:

PKGCFG[0:1] are two external signals used in the CSP package to emulate the different production packages, the status of those signals is normally reflected in the PKG[0-4] field of the SIU MCU ID register (SIU_MIDR). In this silicon revision there is only one configuration allowed: BGA324. Therefore in any calibration solution based on the CSP package, the PKG field is 0b10100 (BGA324) regardless of the package.

Workaround:

The application SW must take into account that, during calibration, the information shown in the MIDR register might not reflect the package under emulation.

1.2 ERR001312: Flash MCR[DONE] bit may be set before high voltage operation completes when executing a suspend sequence

Description:

The program and erase sequence of the flash may be suspended to allow read and program access to the flash core. A suspend operation is initiated by setting the Erase Suspend (ESUS) bit or Program Suspend (PSUS) bit in the flash Module Configuration Register (MCR). Setting a suspend bit causes the flash module to start the sequence which places it in the suspended state. The user must then wait until the MCR[DONE] bit is set before a read or program to the flash is initiated, as the high voltage operation needs to be completed to avoid errors.

However, during normal read to the same partition, following a suspend sequence, (setting MCR bit and waiting for MCR[DONE] bit to be set) can result in read fails that will return multiple bit ECC errors. The error is due to the MCR[DONE] bit being set before the internal high voltage operation is completed.

Workaround:

Because the MCR[DONE] flag can be set too soon, a delay needs to be inserted between setting the MCR[ESUS] or MCR[PSUS] and reading the same flash partition. The minimum duration of the delay should be 40 µs to guarantee the correct operation.

1.3 ERR002382: FLASH: Flash Array Integrity Check

Description:

The Flash Array Integrity Check (AIC) which may be enabled during the flash user test (UTest) mode does not return the expected UMn[MISR] values for some flash PFCRPn[RWSC] read wait state configurations. For PFCRPn[RWSC] values of 3-6, the UMn[MISR] signature computation during AIC does not include the data read from the very last address in the selected address sequence and thus the UMn[MISR] value is not as

expected. For PFCRPn[RWSC] values of 7, the UMn[MISR] signature computation during AIC is not correct as well.

Workaround:

The Flash Array Integrity Check is correct for PFCRPn[RWSC] values of 0-2. For PFCRPn[RWSC] values of 3-6, the expected UMn[MISR] values do not include the data read from the very last address and thus the value expected should be for the data read up to the 2nd-last address in the selected address sequence. For a PFCRPn[RWSC] value of 7, the Array Integrity Check should not be used at all.

1.4 ERR001397 : Reaction Module: Register can set if RAER is asserted

Description:

A modulation can start if the RAER bit is asserted. The REACM_CHSR bit MODACT is asserted.

Workaround:

Enable the RAER interrupt on the module initialization, asserting the REACM_CHCR bit RAEREN. The interrupt service routine must disable the channel, setting the REACM_CHCR field CHEN to zero.

1.5 ERR002740: ETPU2: Watchdog Status Register (WDSR) may fail to update on channel timeout

Description:

The Watchdog Status Register (WDSR) contains a single watchdog status bit for each of the 32 eTPU channels per engine. When this bit is set, it indicates that the corresponding channel encountered a watchdog timeout and was aborted. Under certain conditions the corresponding bit is not set due to a watchdog timeout, and therefore no indication is available as to which channel timed out.

However, the global exception is indicated correctly on a per engine basis, and the correct exception is issued to the interrupt controller and may be serviced.

Workaround:

The application software should treat any watchdog event as a global eTPU exception and handle it in the eTPU global exception handler. Additionally, during the global exception handler the application should check the WDSR and clear any bits that may be set by writing '1' to that bit.

1.6 ERR003221: PMC: SRAM standby power low voltage detect circuit is not accurate

Description:

The power management controller (PMC) SRAM standby voltage low power detect circuit cannot reliably detect the brown-out condition if the standby supply is below 1.0 volt. The

Status Register Brown Out Flag (PMC.SR[LVFSTBY]) bit may not be set during a brownout condition of the SRAM standby voltage or may be set even though no data has been lost.

Workaround:

The application software should not rely on the PMC.SR[LVFSTBY] bit to detect corrupted SRAM values.

1.7 ERR003377: Pad Ring:Nexus pins may drive an unknown value immediately after power up but before the 1st clock edge

Description:

The Nexus Output pins (Message Data outputs 0:15 [MDO] and Message Start/End outputs 0:1 [MSEO]) may drive an unknown value (high or low) immediately after power up but before the 1st clock edge propagates through the device (instead of being weakly pulled low). This may cause high currents if the pins are tied directly to a supply/ground or any low resistance driver (when used as a general purpose input [GPI] in the application).

Workaround:

1. Do not tie the Nexus output pins directly to ground or to a power supply.
2. If these pins are used as GPI, limit the current to the ability of the regulator supply to guarantee the correct start up of the power supply. ELach pin may draw upwards of 150mA.

If not used, the pins may be left unconnected.

1.8 ERR003378: EQADC: Pull devices on differential pins may be enabled for a short period of time during and just after POR

Description:

The programmable pull devices (up and down) on the analog differential inputs of the eQADC may randomly be enabled during the internal Power On Reset (POR) and until the 1st clock edge propagates through the device. After the first clock edge, the pull resistors are disabled until software enables them.

Workaround:

Protect any external devices connected to the differential analog inputs. The worst case condition is with a 1.4 KΩ resistor to VDDA (5K pull-up enabled) or VSSA (5K pull-down enabled). This may also cause temporary additional current requirements on the VDDA supply of each eQADC module, up to 15 mA on each eQADC if both the pull up and pull down resistors are enabled simultaneously on all of the differential analog pins.

1.9 ERR003407: FlexCAN: CAN Transmitter Stall in case of no Remote Frame in response to Tx packet with RTR=1

Description:

FlexCAN does not transmit an expected message when the same node detects an incoming Remote Request message asking for any remote answer.

The issue happens when two specific conditions occur:

1. The Message Buffer (MB) configured for remote answer (with code "a") is the last MB. The last MB is specified by Maximum MB field in the Module Configuration Register (MCR[MAXMB]).
2. The incoming Remote Request message does not match its ID against the last MB ID.

While an incoming Remote Request message is being received, the FlexCAN also scans the transmit (Tx) MBs to select the one with the highest priority for the next bus arbitration. It is expected that by the Intermission field it ends up with a selected candidate (winner). The coincidence of conditions (1) and (2) above creates an internal corner case that cancels the Tx winner and therefore no message will be selected for transmission in the next frame. This gives the appearance that the FlexCAN transmitter is stalled or "stops transmitting".

The problem can be detectable only if the message traffic ceases and the CAN bus enters into Idle state after the described sequence of events.

There is NO ISSUE if any of the conditions below holds:

a) The incoming message matches the remote answer MB with code "a".
b) The MB configured as remote answer with code "a" is not the last one.
c) Any MB (despite of being Tx or Rx) is reconfigured (by writing its CS field) just after the Intermission field.
d) A new incoming message sent by any external node starts just after the Intermission field.

Workaround:

Do not configure the last MB as a Remote Answer (with code "a").

1.10 ERR003659: FLASH: Resuming after a suspend during an Erase may prevent the erase from completing

Description:

If an erase suspend (including the flash put into sleep or disabled mode) is done on any block in the low Address Space (LAS) or the Mid-Address Space (MAS) except the 16KB blocks, or if a suspend is done with multiple non-adjacent blocks (including the High Address Space [HAS]), the flash state machine may not set the FLASH_MCR[DONE] bit in the flash Module Control Register. This condition only occurs if the suspend occurs during certain internal flash erase operations. The likelihood of an issue occurring is reduced by limiting the frequency of suspending the erase operation.

Workaround:

If the suspend feature (including disable and sleep modes) of the flash is used, then software should ensure that if the maximum time allowed for an erase operation occurs without a valid completion flag from the flash (FLASH_MCR[DONE] = 1), the software

should abort the erase operation (by first clearing the Enable High Voltage (FLASH_MCR[EHV]) bit, then clearing the Erase read/Write bit (FLASH_MCR[ERS] bit) and the erase operation should be restarted.

Note: The cycle count of the sector is increased by this abort and restart operation.

1.11 ERR004480 eQADC: Differential conversions with 4x gain may halt command processing

Description:

If the four times amplifier is enabled for a differential analog-to-digital conversion in the Enhanced Queued Analog to Digital Converter (eQADC) and the ADC clock prescaler is set to divide by 12 or greater, then the ADC will stop processing commands if a conversion command is executed immediately after a differential, gain 4x conversion.

Workaround:

1. Do not use a prescaler divide factor greater than or equal to 12 (11 can be used on devices that support odd prescalers).
2. Insert a dummy write command to any internal ADC register after every 4x conversion command.

Note: If the command FIFO preemption feature is used and it is possible to preempt a FIFO which contains the 4x conversion + dummy write workaround, then the preempting command FIFO must be loaded FIRST with a dummy write command and then the desired preempting conversion command in order to avoid the possibility of following a 4x conversion command with another conversion command in the same ADC.

The level sensitive triggers (when in Low/High Level Gated External Trigger, Single/Continuous Scan modes) can interrupt the command sequence at any point in time, potentially breaking the safe sequence 4x conversion command -> dummy write command.

When using an odd prescaler (ADCx_CLK_ODD = 1), the duty cycle setting (ADCxCLK_DTY) must be kept at the default setting of 0.

1.12 ERR004532:REACM: OCDF flag is set during hold-off time

Description:

The Reaction Modules (REACM) Open Circuit Detection Flag (OCDF) indicates that an Open Circuit was detected during the holdoff time phase of a threshold-holdoff modulation. This flag indication is incorrect because the OCDF flag is meant to indicates ON periods larger than a configured value. In this case, OCDF is setting during the OFF phase of the modulation.

Workaround:

When a modulation sequence has a phase that uses Threshold-holdoff modulation mode, the OCDF flag cannot be used reliably. In is this case, one can write the Modulation Range Pulse Width Register [REACM_RANGEPWD] register to '0x000' which will disable the check of "Open Circuit" functionality.

2 Errata summary

Table 2. Errata list

Old defect ID	Defect ID	Errata Title	cut 1.0	cut 1.1	cut 2.0
e6196PS	ERR003108	NPC: Auxiliary Trace output limited to 25 MHz	X	X	
e6701PS	ERR003138	PMC: Internal 3.3V Regulator Issues and Considerations	X		
e6817PS	ERR003148	SIU: Wrong supply information shown in the MIDR2 register	X		
e7204PS	ERR003170	JTAG: Low swing mode of JTAG and Nexus signals is not functional in the QFP176 package	X		
e7205PS	ERR003171	e200z4: Instruction Cache is not functional	X		
e7253PS	ERR003173	Pad ring: AN8 and AN38 swapped	X	X	
e7333PS	ERR003177	Temperature Sensor: wrong supply	X	X	
e8804PS	ERR003227	NEXUS: MCKO divide by 3 not functional	X	X	
e8962PS	ERR003238	ECSM: ECC single bit error reporting not available	X	X	
e6852073PDM	ERR002424	FlexCAN: switching CAN protocol interface (CPI) to system clock has very small chance of causing the CPI to enter an indeterminate state	X	X	
e6860916PDM	ERR001741	EQADC : 25% calibration channel sampling requires at least 64 sampling cycles	X	X	(1)
e6877374PDM	ERR000652	EQADC: 50% reference channels reads 20 mv low	X	X	(1)
e8773PS	ERR003221	PMC: SRAM standby power low voltage detect circuit is not accurate	X	X	X
e5116PS	ERR003050	e200z4: 16-bit VLE Conditional Branch can give unexpected results	X	X	
e6863118PDM	ERR001284	FLASH: Incorrect Prefetch at the end of Bank0 boundary (to Bank1)	X	X	
e6873750PDM	ERR002382	FLASH: Flash Array Integrity Check	X	X	X
e6867455PDM	ERR001312	FLASH: MCR[DONE] bit may be set before high voltage operation completes when executing a suspend sequence	X	X	X
e6850448PDM	ERR000575	DSPI: Changing CTARs between frames in continuous PCS mode causes error	X	X	
e6858450PDM	ERR001103	DSPI: PCS Continuous Selection Format limitation	X	X	
e6856645PDM	ERR001267	DSPI: DSPI Microsecond Bus Limitations	X	X	
e6869199PDM	ERR002347	eSCI: LIN Receive Register cleared before data has been read	X	X	
e6875199PDM	ERR002386	eSCI : No LIN frame reception after leaving stop mode	X	X	
e6849526PDM	ERR002396	eSCI : Stop Mode not entered in LIN mode	X	X	
e6847076PDM	ERR001171	eSCI : DMA stalled after return from stop or doze mode	X	X	
e6870961PDM	ERR001221	eSCI: LIN bit error indicated at start of transmission after LIN reset	X	X	

Table 2. Errata list (continued)

Old defect ID	Defect ID	Errata Title	cut 1.0	cut 1.1	cut 2.0
e6864631PDM	ERR001297	eSCI : reads of the SCI Data Register, which clears the RDRF flag, may cause loss of frame if read occurs during reception of the STOP bit	X	X	
e6976403PDM	ERR001381	eSCI: LIN Wakeup flag set after aborted LIN frame transmission	X	X	
e6886033PDM	ERR001364	FlexRay : Message Buffer Slot Status corrupted after system memory access timeout or illegal address access	X	X	(1)
e6949905PDM	ERR001369	FlexRay : Message Buffer Status, Slot Status, and Data not updated after system memory access timeout or illegal address access	X	X	(1)
e6847364PDM	ERR001339	eTPU: MRL Branch Condition at the start of the thread may differ from the actual MRL state if channel runs at full speed	X	X	
e6865252PDM	ERR002338	Pad Ring: Leakage if VDDE is greater than VDD33	X	X	
e5445PS	ERR003067	Pad Ring: Pins with LVDS input have interaction if current is injected on one pin	X	X	
e8775PS	ERR003222	DSPI: LVDS pads VOS (Common mode voltage) out of specification	X	X	
e6862439PDM	ERR001779	SIU: CRSE bit added to the SIU Configuration Register	X	X	
e6895076PDM	ERR001397	Reaction Module: Register can set if RAER is asserted			X
e9631PS	ERR003285	SIU: MCU ID register package information not reliable on the calibration package	X	X	X
e6854906PDM	ERR001419	SIU: Reverting ENGCLK source to the system clock has a very small chance of causing the ENGCLK generator to enter an indeterminate state	X	X	
e6858715PDM	ERR002423	FlexRay: Transmission in a slot n of Channel A in dynamic segment may be corrupted or duplicated on both the channels	X	X	(1)
e6859837PDM	ERR001322	FlexRay : Error Injection enabled independent of MCR[ECCE]	X	X	(1)
e12982697PDM	ERR002449	EQADC: Conversions can be inaccurate when only one ADC is enabled	X	X	(1)
e6880216PDM	ERR001363	e200z4: mtlr followed by se_rfi/se_rfci/se_rfdi/se_rfmci can give unexpected results	X	X	
e6887863PDM	ERR000817	JTAGC: EVTI and RDY require TCK to toggle	X	X	
e6878253PDM	ERR001433	Flash: UMISRx not writable after running user margin read	X	X	(1)
e6183PS	ERR003105	DSPI: Correct programming of frames in Tx FIFO in master and slave mode.	X	X	(1)
e8845PS	ERR003230	DSPI: Correct usage for Tx FIFO when continuous clock mode is enabled	X	X	(1)
e6861055PDM	ERR001082	DSPI: set up enough ASC time when MTFE=1 and CPHA=1	X	X	
e6871272PDM	ERR002360	FlexCAN: Global Masks misalignment	X	X	(1)
e6853852PDM	ERR002421	FLEXRAY: Message Buffer cannot be disabled in POC state INTEGRATION_LISTEN			(1)

Table 2. Errata list (continued)

Old defect ID	Defect ID	Errata Title	cut 1.0	cut 1.1	cut 2.0
e9586PS	ERR003274	REACM: Reaction Channels are not available	X	X	
e9587PS	ERR003275	Decimation Filter: features not available	X	X	
e9588PS	ERR003276	DSPI: Micro Second Channel (MSC) and Parity generation/checking not available	X	X	
e9589PS	ERR003277	DTS: module not available	X	X	
e9610PS	ERR003278	e200z4: Cache size is 4K	X	X	
e9611PS	ERR003279	e200z4: Only 16-entry MMU available	X	X	
e9612PS	ERR003280	Pbridge: access control not available	X	X	
e9613PS	ERR003281	MPC564xA/SPC564A: Maximum Frequency limited to 145 MHz	X	X	
e9617PS	ERR003284	SIU: Realtime MMU alteration feature not available	X	X	
e9762PS	ERR003296	SIU: signals not available	X	X	
e9615PS	ERR003283	eQADC: STAC bus import to ADC and use of odd prescalers are not available	X	X	
—	ERR002740	ETPU2: Watchdog Status Register (WDSR) may fail to update on channel timeout			X
—	ERR003377	Pad Ring:Nexus pins may drive an unknown value immediately after power up but before the 1st clock edge			X
—	ERR003378	EQADC: Pull devices on differential pins may be enabled for a short period of time during and just after POR			X
—	ERR003407	FlexCAN: CAN Transmitter Stall in case of no Remote Frame in response to Tx packet with RTR=1			X
—	ERR003659	FLASH: Resuming after a suspend during an Erase may prevent the erase from completing			X
—	ERR004480	eQADC: Differential conversions with 4x gain may halt command processing			X
—	ERR004532	REACM: OCDF flag is set during hold-off time			X

1. Described in the RM0029 rev 5 (see *Section A.1: Reference document*).

Appendix A Further information

A.1 Reference document

1. *SPC564A80B4, SPC564A80L7 32-bit MCU family built on the* embedded Power Architecture® (RM0029, Doc ID 15177).
2. *32-bit MCU family built on the embedded Power Architecture®* (SPC564A74B4, SPC564A74L7, SPC564A80B4, SPC564A80L7 datasheet, Doc ID 15399).

A.2 Acronyms

Table 3. Acronyms

Acronym	Name
ADC	Analog-to-digital converter
AIC	Array integrity check
CDACNTL	Cache debug access control register
CDADATA	Cache debug access data register
CDFC	Channel digital filter control
CHIERFR	Controller host interface error flag register
CTAR	Clock and transfer attribute registers
CRSE	Calibration reflection suppression enable
DMA	Direct memory access
DSI	Deserial serial interface
EDF	Enhanced digital filter
eSCI_LRR	eSCI LIN receive register
eQADC	Enhanced queued analog-to-digital converter
ETPUECR	eTPU engine configuration register
FCSS	Filter clock source selection
FIFO	First in first out
ILSA_EF	illegal system bus address error flag
LOC	Loss-of-clock
LVD	Low voltage detector
LVDS	Low voltage differential signalling
LST	Long sample time
MB	Message buffer
MCKO	Nexus clock
MCR	Module configuration register
MIDR	MCU ID register

Table 3. Acronyms (continued)

Acronym	Name
MDO	Nexus message data output
ME	Match enabled
MRL	Match recognition latch
PCR	Pad configuration register
PFAPR	Platform Flash access protection register
PFCR	Platform Flash configuration register
RDRF	Receive data register full
RXGMASK	RX global mask
RXIMR	RX individual mask register
SBCF_EF	System bus communication failure error flag
SCI	Serial communications interface
SCISR	SCI status register
SIU_DISR	DSPI input select register
TST	Time slot transition
VRH	High reference voltage
VRL	Low reference voltage

Revision history

Table 4. Document revision history

Date	Revision	Changes
01-Feb-2011	1	Initial release.
03-Feb-2011	2	Updated JTAG_ID. Updated *Table 2: Errata list*
03-Nov-2011	3	Renamed following functional problems: – e9631 PS with ERR003285 – e6867455 PDM with ERR001312 – e6873750 PDM with ERR002382 – e6895076 PDM with ERR001397 Added following functional problems: – ERR002740 – ERR003221 – ERR003377 – ERR003378 – ERR003407 – ERR003659 Removed following functional problems: – e6859837 PDM – e6865252 PDM – e6860916 PDM – e6877374 PDM – e12982697 PDM – e6880216 PDM – e6887863 PDM – e6878253 PDM – e6183 PS – e8845 PS – e6853852 PDM – e6858715 PDM – e6886033 PDM – e6949905 PDM – e6871272 PDM Updated *Table 2: Errata list*
16-Mar-2012	4	Added following functional problems: – ERR004480 – ERR004532 Updated *Table 2: Errata list*
02-Oct-2012	5	Added RPNs SPC564A74L7 and SPC564A74B4. Changed the title. Updated *Table 1: Device summary* Updated *Section A.1: Reference document*
18-Sep-2013	6	Updated disclaimer.

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