NavChip™ Interface Control Document (ICD)
(And InertiaCube*NC* Products)

Firmware 1.155 and later

Revision history:

Rev	Date	Firmware	Comments
1	2015-05-15	1.152	Preliminary release
2	2015-07-15	1.155	Updated register map to include magnetometer registers
3	2015-08-06	1.155	Corrected register description of calibration date parsing

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1 Introduction

This document defines the protocol interface of the NavChip with the host system. Electrical and mechanical interfaces are described separately in the NavChip datasheet, which should be used in conjunction with this ICD. This NavChip interface control document fully describes the NavChip packet structure and all commands, responses and output data packet formats that are applicable to the NavChip.

The NavChip commands and responses are listed in Table 9 in Section 3.3. For basic operation, one needs only to apply power, and then send the Start Streaming command, which will cause the NavChip to start streaming out the default data packet type (type 3) at the default data rate (200 Hz). Optionally, before entering streaming mode, the Set Register command can be used to configure a different output data packet type, data rate, baud rate, etc. The output data packet types are documented in Section 3.5, and currently includes two pre-set data packet formats.

2 NavChip interfaces and modes

2.1 Interfaces

NavChip supports UART and SPI interfaces for communications with external systems, operating at 3V TTL levels. All commands, acknowledgements and data packet messages operate identically for both the interfaces. It is possible to switch between the interfaces to execute commands, but commands should not be sent on both of the interfaces at the same time. To switch between interfaces, simply send any command on an interface, and it will switch to the active interface. The default interface is the UART (the default interface is used when streaming data on start-up, though the NavChip automatically switches between interfaces whenever it receives data on a given interface).

2.1.1 UART interface

The NavChip UART external communication interface is a full-duplex serial communication port. The default baud rate is 115,200 bps with 1 start bit, 1 stop bit, and no parity. The UART receives commands on the RX pin, and transmits outgoing messages on the TX pin, including both command replies and streaming data packets.

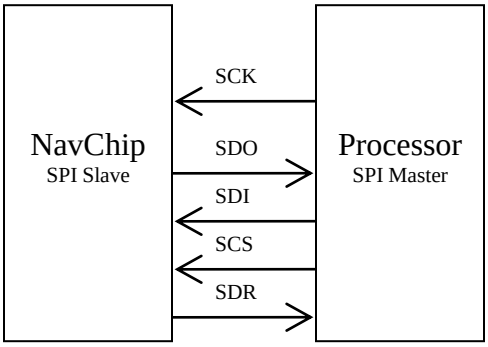
2.1.2 SPI interface

The NavChip also supports SPI based communication with external systems and operates in slave mode. The SPI interface includes SPI clock (SCK), SPI data-out (SDO), SPI data-in (SDI), and SPI chip-select (SCS) signals for communication as well as serial data ready (SDR) signal for handshake. The serial data ready (SDR) signal transitions from low to high when a new data packet or command acknowledgement is loaded into the buffer and ready to be clocked out by the master device. The SPI chip select (SCS) line is

used to select the SPI port, the SPI peripheral clocks out the data only when the SCS line is low.

Table 1: SPI signal descriptions

Signal name	Description
SCK	SPI serial clock
SDO	SPI data output
SDI	SPI data In
SCS	SPI chip select
SDR	SPI data ready



The data ready signal goes low once all the data in the buffer is clocked out and stays low until a new data packet or command acknowledgement is available in the transmission buffer. If the host does not clock out the current data packet, it will be discarded and the SDR line will go low for approximately 50 μs before new data is ready, so every new data packet will generate a rising edge on SDR which can be used to interrupt the host controller.

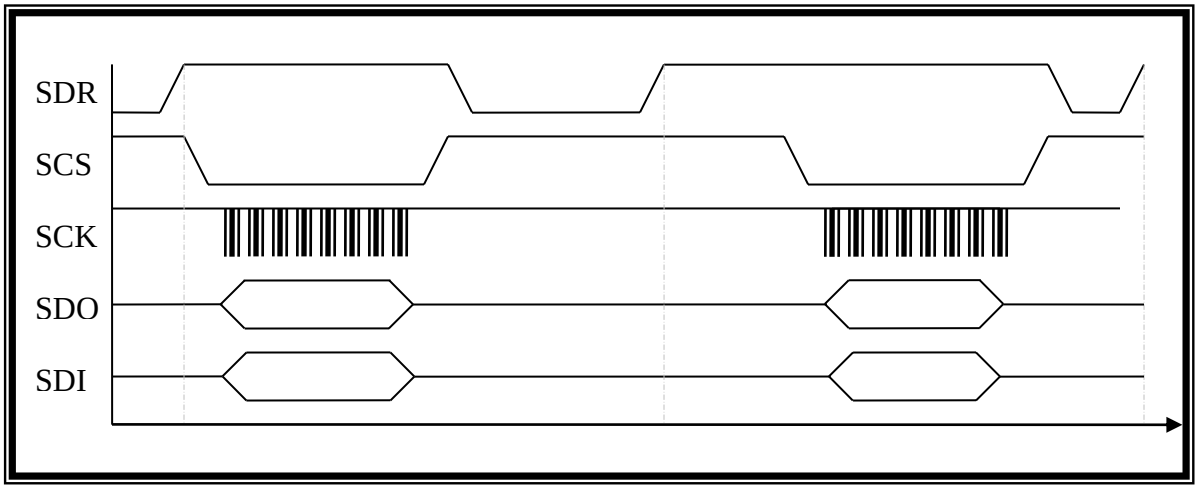


Figure 1: SPI packet timing diagram

The serial peripheral interface (SPI) port is configured as a SPI slave and the data can be clocked out at rates up to 8 Mbps. The SPI port is configured so that the idle state for the master clock is a high level (clock polarity, CPOL=1). Data is read from SDO/written to SDI by the SPI master on the rising edge (clock phase, CPHA=1). The data to/from the

SPI port is formatted in 8-bit big endian words. SCS may either remain low between bytes, or toggle high as shown by the dotted lines in Figure 2.

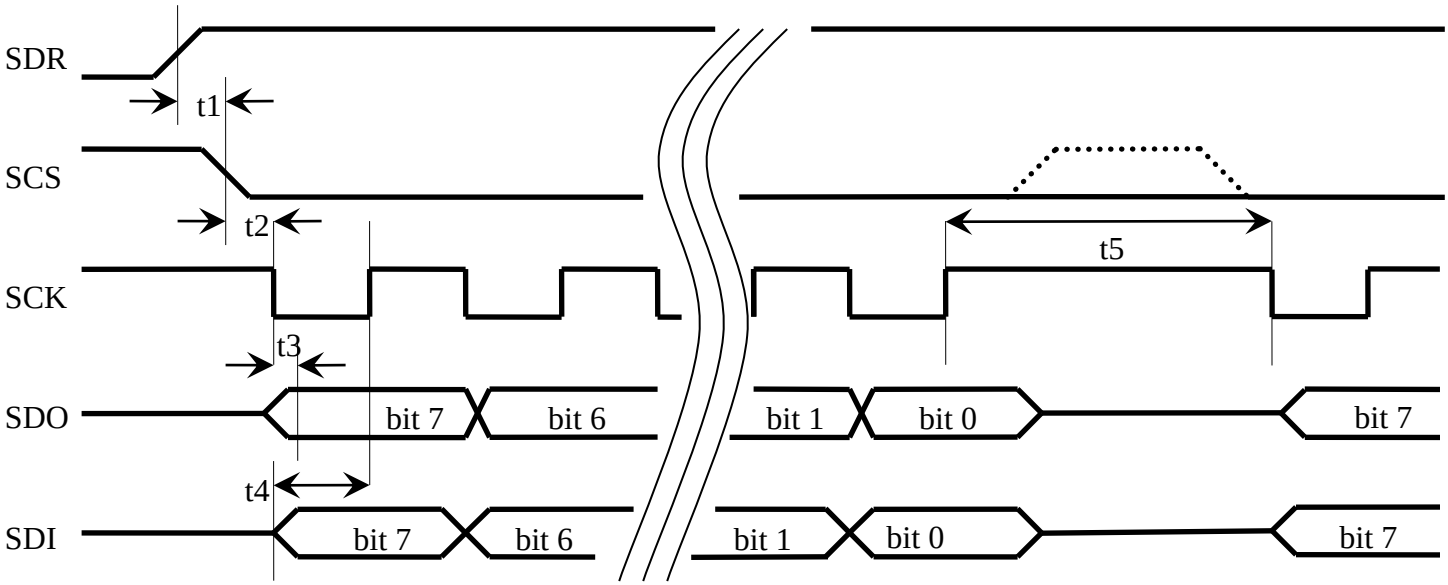


Figure 2: SPI byte timing diagram

Table 2: SPI timing

Parameter	Description	Value		Units
		Min	Max	
f_{SCK}	SPI serial clock frequency		8	MHz
t_1	Data ready(SDR) to chip select (SCS) time	25		ns
t_2	Chip select(SCS) to clock edge (SCK) time	25		ns
t_3	Clock edge(SCK) to output bit stable (SDO) time	25		ns
t_4	SDI setup time before clock edge(SCK)	65		ns
t_5	Inter-byte delay	200		ns

2.2 Synchronization

NavChip has the capability to synchronize its data sampling to an external rising edge signal applied at the Sync pin. If the sync function is not turned on, or the sync signal is not exercised, the NavChip will free-run and output data packets at the specified rate, with a clock accuracy of ±20 ppm. When the sync function is enabled, the sync signal can be used to synchronize the NavChip's internal 1 KHz data acquisition, processing and transmission to an external signal.

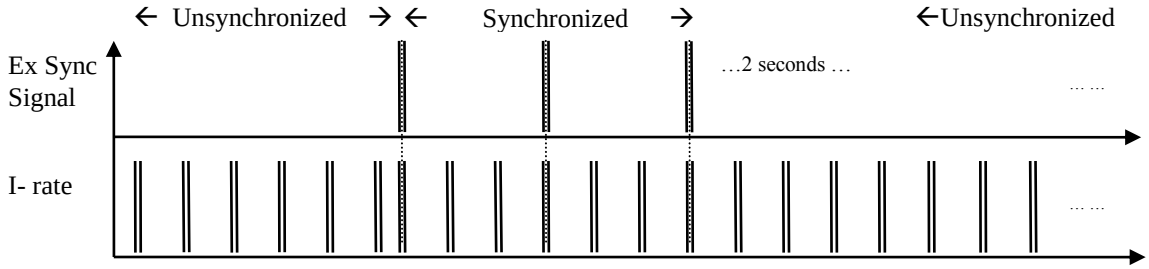


Figure 3: External synchronization timing diagram

Sync pulses may be sent to the NavChip at any rate whose period, P, is an integer number of milliseconds. The external sync source must have a clock drift less than 20 microseconds over the period P. Each received sync pulse will cause the NavChip to adjust its internal data acquisition timer to match the external clock. Once synchronized, sync pulses that fall outside of the ±20 μs boundary will be ignored. Sync pulses must be received at least once every second in order to keep the NavChip "in sync". After two seconds without acceptable pulses, the NavChip will be "out of sync", and the next received pulse will re-initialize the synchronization, which may cause the CBIT of the data to fail on that cycle. If the sync rate is an integer multiple of the data transmission rate and the system remains in sync, then the data transmission times will continue to have the same phase relative to the sync pulse on each sync cycle. The NavChip triggers on the rising edge of the sync pulse.

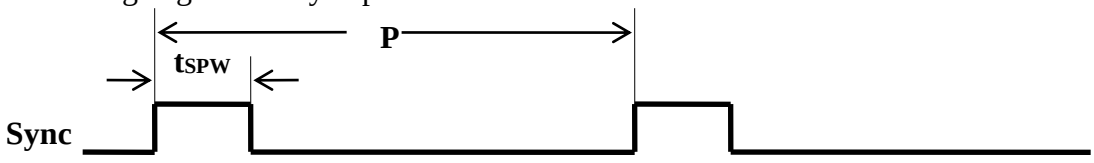


Figure 4: External Sync timing

Table 3: External Sync timing

Parameter	Description	Value		Units
		Min	Max	
t_{SPW}	Sync pulse (positive) width	0.01	900	us
P	Sync pulse period (integer milliseconds)	1	1,000	ms

2.3 Modes

The NavChip implements a partitioned firmware for operation in **Bootloader Mode** and **Operating Mode**. Figure 5 illustrates the different modes and possible transition paths between them.

2.3.1 Bootloader Mode

NavChip has a capability to perform a firmware upgrade in the field. On power-up the NavChip executes a ½ second Delay Boot Mode where it is waiting for either a Ping command to exit Bootloader Mode and jump to Operating Mode or a Firmware Upgrade command to jump to Firmware Upgrade Mode. Firmware upgrade in the field can be performed by customers using a Thales Visionix provided upgrade utility, such as *Hardware Diagnostics* or *DeviceTool2*.

2.3.2 Operating Mode

Once the NavChip exits the ½ second Delay Boot Mode it enters Startup Mode where it initializes the hardware and performs quick built-in-tests (QBIT) on the sensors. NavChip has two other modes of operation, Standby Mode and Streaming Mode. In Streaming Mode, the NavChip actively acquires data from the sensors and transmits data. In Standby Mode, the NavChip performs the same acquisition and processing in order to stabilize the temperature while it waits for external commands, but does not stream output data. Refer to Table 4 for typical start-up sequence and timing.

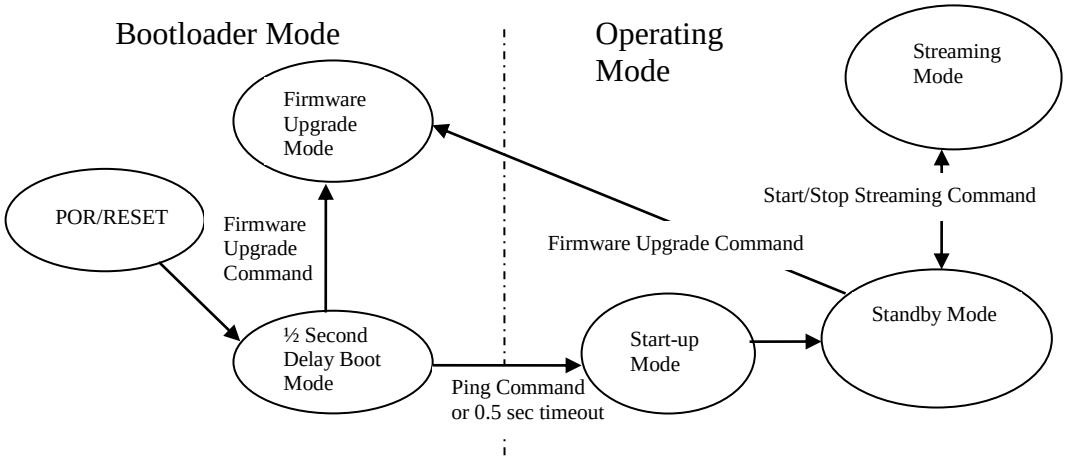


Figure 5: NavChip mode transition diagram

Table 4: NavChip start-up sequence timing

Time (ms)	NavChip Status	Comment
0	Power applied	½ second delay boot starts
T_1 (max 500)	Switch from bootloader to Startup Mode	T_1=500 ms, or earlier if Ping command received.
T_1+200	Switch from Startup Mode to Standby Mode	Hardware initialized, QBIT complete, ready to stream valid data
$T_2 > T_1 + 200$	Enter Streaming Mode	By default, T_2 is the time when Start Streaming command is received. If auto-streaming parameter has been configured and saved, the device will automatically switch to streaming mode upon completion of startup mode, and $T_2=T_1+200$.

3 Communications protocol

3.1 Packet structure

Commands begin with a start byte and a header byte, formatted as shown in Table 5. Some commands include a body, typically containing additional command parameters and data. A checksum is added to the end of the command. The checksum is the two's complement of the sum of all preceding bytes including the start byte and header. Little-endian format is used for multi-byte words for communication and addressing within the NavChip. All signed integers use the two's complement format.

3.1.1 Command packet structure

The *start byte* is always 0xA5. The *header* byte consists of an *address* nibble and a *command* nibble.

Address specifies the recipient device; in the future a feature may be added to allow up to 8 unique devices to communicate on a single communication port. Until then, there is no reason to change the address from its default value of zero.

Table 5: Command packet structure

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xA				0x5			
Spare	Address (0-7)			Command (0-15)			
Body (command-dependent)							
Checksum							

The commands supported by the NavChip are listed in Table 9.

3.1.2 Reply packet structure

Replies start with an echo of the command header byte and may be followed by additional data bytes depending on the command. Replies that include a body (typically containing data) also have a checksum appended, which includes all preceding bytes.

Table 6: Reply packet structure

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Command header echo							
Reply data byte(s)*							
Checksum*							
Note: *Present only when reply includes a body.							

3.2 Data and baud rates

The NavChip always updates internally at exactly 1000 Hz (+/- 0.05 Hz). It can transmit the data at any of the following submultiples:

Table 7: NavChip data output rate

data rate = data rate max/divisor	
data rate divisor	**output data rate**
5	**200.000 Hz (default)**
6	166.667 Hz
7	142.857 Hz
8	125.000 Hz
9	111.111 Hz
10	100.000 Hz

For packets containing $\Delta\theta$ and $\Delta\mathbf{V}$ data, the minimum supported data rate is 100 Hz.

Communication can occur at a maximum baud rate of 921,600 or any of the following submultiples listed in Table 8. Other divisors will not be rejected (and will set the baud rate to the expected rate), but only the divisors listed in Table 8 are officially supported (they are guaranteed to have under 1% error from the actual rate).

Table 8: NavChip baud rates

baud rate = baud rate max/divisor	
baud rate divisor	**output baud rate**
1	921,600 (Max)
2	460,800
4	230,400
8	**115,200 (default)**
24	38,400

Beware when programming the communications parameters that the baud rate must be high enough to support the chosen data rate and packet type combination. For a packet type with total length N bytes, the length will be 10*N bits (including the start and stop bit), so the baud rate should be at least 20% higher than 10*N*data rate. If not, the NavChip will drop data packets whenever the serial port transmission cannot keep up with the rate at which new data is being generated. Higher data rates will cause the NavChip to draw more current (consult the datasheet for details).

3.3 NavChip command set

Please refer to the key below for notation frequently used in the command syntax.

Key:

<s>	Start byte *s*=0xA5
<ax>	Header byte where *a*=device address, *x*=command
<d>	Data byte
<ct>	Total number of bytes in a command, including header and checksum
<cs>	Checksum byte (negative sum of all preceding bytes)
<ma>	Represents a register address

For example, the command to obtain the results of register 0 would be the four hex-format bytes A5 01 00 5A (the get register format is <s><a1><ma><cs>).

Note that a small number of simple commands are used to interface with and control the NavChip, and that all configuration is performed by setting registers. Configuration and status information can be obtained by reading registers directly, or via information streamed out along with the data itself in data packets.

Streaming status includes the presence or absence of a fault condition, the magnetometer axis being reported (for devices with magnetometers), and an "S" bit in the discrete status byte (see Table 10) that may be used to construct registers 0-31 after a complete frame (256 records). These registers include a temperature register, runtime warning flags and synchronization status.

Table 9: NavChip command set

Command	Command Syntax	Reply Syntax
Ping/Stop Streaming	<s><a0><cs>	<a0> if not streaming, else stops streaming but no reply.
Get Register[1,2]	<s><a1><ma><cs> Refer to sections 4.1 and 4.2 for meaning of the bytes of the Configuration Registers. $0 \leq ma \leq 255$	<a1><d><cs>
Set Register[1,2]	<s><a2><ma><d><cs> Refer to sections 4.1 and 4.2 for meaning of the bytes of the Configuration Registers. $0 \leq ma \leq 255$ Set the address *ma* to 0xFF and *d* to 0 to save the updated data to FLASH memory. Set the address *ma* to 0xFF and *d* to 1 to restore all registers to default values. These values are only in RAM until they are saved to FLASH, but take effect immediately.	<a2> A valid acknowledgement means the set register data is valid and was applied to the system successfully.
Start Streaming	<s><a5><cs> Starts streaming data packets, or continue streaming if the Stream Timeout register, 159 (0x9F), is used. No command acknowledgement is given for this or any other command while streaming. Use the ping command to stop streaming.	No reply.
Diagnostics[2]	<s><a8><ct><cs> Causes NavChip to execute Thorough Built-In Tests (TBIT). Results are read back from configuration register set locations 36-42.	<a8> May take a second or more to complete tests and acknowledge.

Notes:

1. These commands will read and update the RAM copy of flash memory. All updates should be made to the RAM copy, and then saved to flash (if desired) once completed. Changes will be lost upon power cycling the NavChip, unless they are saved to flash memory.
2. This commands are not available in Streaming Mode. They will be ignored if accidentally sent.

All commands except Diagnostics and Set Register (with <ma> = 0xFF) will execute within 5 milliseconds. Invalid commands or commands with invalid parameters are not executed or acknowledged.

3.4 Error/status reporting (QBIT/TBIT/CBIT)

The NavChip has several mechanisms for reporting errors: QBIT (Quick Built-In Test), CBIT (Continuous Built-In Test) and TBIT (Thorough Built-In Test). Once performed, tests provide results by setting the discrete flag byte (register 89) "F" flag and updating Configuration Registers 36-42 to provide details of the problem.

CBIT results persist until the end of the frame in which they appear (up to 256 packets, depending on the packet ID when they first appear). The specific packet which contains the CBIT error is indicated by the fault ("F") flag in the packet. The CBIT results are cleared at the start of each frame. These tests update registers 38-39 (0x26-0x27).

TBIT, initiated with the Diagnostic command, performs a detailed test of all internal sensors and system parameters. TBIT is able to detect serious issues with the internal sensors, such as mechanical or electrical failures, though it does require the sensor to be stationary in order to accurately report failures. If failures are indicated, please provide a brief logged data file (which includes all registers) to allow Technical Support to assist in troubleshooting the issue. These tests update registers 36-37 (0x24-0x25) and 40-42 (0x28-0x2A).

QBIT, the quick built-in tests, are always run once upon initialization, and only check for basic issues that can be detected very quickly. These tests update registers 36-37 (0x24-0x25) and 40-42 (0x28-0x2A).

3.5 Packet Data Items

3.5.1 PacketID

PacketID is an 8-bit sequence counter of the packet number relative to the start of this 256-record data frame. This can be used to decode the Configuration Registers one bit or one byte at a time during streaming mode (see the S flag description in Table 10).

3.5.2 Packet Transmission Latency (PTL)

Packet Transmission Latency is a 16-bit value that represents the time in microseconds since the end of the last data integration period (whose integral is being transmitted in this packet). If the NavChip has run continuously with no changes of RateDivisor, time since start will be:

$$\text{Time } (\mu s) = (\text{FrameID}*256 + \text{PacketID})*\text{RateDivisor}*1000 + \text{PTL}$$

The PTL value is a 16-bit signed integer, so it represents approximately ±32,768 µs. Normally, it represents the transmission time of the packet, which is always AFTER the end of the data integration period, so it will be a positive number. The packet is transmitted at the end of the third i-rate integration period following the end of the integration period to which it corresponds. This implies that the latency of reporting is 3 ms plus the latency of communicating the selected packet size at the selected baud rate.

3.5.3 DeltaTheta

DeltaTheta is an incremental rotation vector over the data integration period, including coning compensation if enabled. Angular integrals are maintained internally with higher precision, and any truncated remainders are carried forward and added to the next output packet, so that numerical round-off will not affect the long-term integration accuracy.

Each bit represents 0.00625 mrad, with ±32768 bits range, so the maximum rotation per update period is 0.2048 rad. In a high-dynamic application with angular rates up to 20 rad/s, the update rate must be at least 100 Hz to prevent overflow.

3.5.4 DeltaV

DeltaV is an integral of accelerometer measurements over the data integration period, including coning and sculling compensation if enabled. Velocity integrals are maintained internally with higher precision, and any truncated remainders are carried forward and added to the next output packet, so that numerical round-off will not affect the long-term integration accuracy.

Each bit represents 39.0625e-6 m/s, with ±32768 bits range, so the maximum velocity change per update period is 1.28 m/s. In a high dynamic application with linear accelerations up to the maximum 120 m/s/s that the NavChip can measure, the update rate must be at least 100 Hz to prevent overflow.

3.5.5 Mag_I

Mag_I is the compensated magnetic measurement in Gauss for the I^{th} axis. The value of *I* increments to indicate that X (*I*=1), Y (*I*=2) and Z (*I*=3) axis data is included in the packet, as new data is being acquired from the magnetometer sensor. When no new data is available, or in NavChips that do not contain magnetometers, $I = 0$ and $\boldsymbol{Mag_I} = 0$.
Each bit represents 0.25e-3 Gauss with ±32768 bits range, so the maximum measurement range is +/-8.192 Gauss. The index *I* which specifies the current axis is contained in byte 3 (the 4^{th} byte) of the packet, the discrete flag byte.

NOTE: Currently, only the InertiaCube*NC* product line has magnetometers.

3.5.6 Discrete flag byte

The discrete flag byte provides status information, and is output in both packet types 3 and 4. It allows the first 32 registers to be read out at a low rate while streaming data, provides information about hardware or other faults, and provides an index to the currently reported magnetometer axis for NavChips and NavChip-based devices that are equipped with magnetometers.

Table 10: Discrete flag byte description

Item Name	Bits	Description
R7	7	Reserved for future use.
R6	6	Reserved for future use.
D	5	Reserved for future use.
S	4	The *S* flag represents the value of the n^{th} bit of the 256-bit Configuration Registers, where n is the PacketID. Therefore, the Configuration Registers get played out once per 256-record frame, reading one bit at a time from byte 0/bit 0 to byte 31/bit 7. The receiving software can reconstruct Configuration Registers 0-31 after each 256 records (e.g. once every 1.28 seconds at the default 200Hz data rate) if all packets are received during that time.
F	3	The *F* flag signals a fault condition. The F flag will be high if there are any runtime warning flags (refer to the RUNTIME_WARN register (23) for more information).
R2	2	Reserved for future use.
I	1:0	Index of **MagI**

3.6 Boresight matrix

Configuration Registers 44 – 61 allow for a user-provided boresight matrix to be applied to NavChip output data. This is important to set when the NavChip is mounted inside a housing, since it will allow the NavChip to produce output in the housing's frame of reference instead of the NavChip's. The *Hardware Diagnostics* utility includes functionality to calculate this matrix if the NavChip is mounted in a housing that has flat surfaces on the housing's Y and Z axes. Please see the Configuration Register Details section for more information about the format of the Matrix (each 2-byte matrix element is a 16-bit signed value with a resolution of 1/32768, or 3.05176e-5).

3.7 Data Packet Types

The NavChip supports a variety of different Data Packets which are user-selectable for different applications. The default is Packet Type 3. Choosing a packet type through the Set Register command causes the NavChip to perform the necessary algorithms and computations to provide the selected type of output data. Only one type of data packet may be streamed at a given time.

3.7.1 Packet Type 3: Compensated Δθ and ΔV (default)

Table 11: NavChip Packet Type 3

Byte No.	contents							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Start byte (0x*a*5, a = device address)							
1	Data Packet Type (0x03)							
2	PacketID bits 7-0							
3	E1	E2	D	S	F	R	I	
4	Packet Tx Latency bits 7-0							
5	Packet Tx Latency bits 15-8							
6	$DeltaV_x$ bits 7-0							
7	$DeltaV_x$ bits 15-8							
8	$DeltaV_y$ bits 7-0							
9	$DeltaV_y$ bits 15-8							
10	$DeltaV_z$ bits 7-0							
11	$DeltaV_z$ bits 15-8							
12	$DeltaTheta_x$ bits 7-0							
13	$DeltaTheta_x$ bits 15-8							
14	$DeltaTheta_y$ bits 7-0							
15	$DeltaTheta_y$ bits 15-8							
16	$DeltaTheta_z$ bits 7-0							
17	$DeltaTheta_z$ bits 15-8							
18	Checksum bytes 0-17							
Note: For information on data items, please refer to section 3.5.								

3.7.2 Packet Type 4: Compensated Δθ, ΔV and M

Table 12: NavChip Packet Type 4

Byte No.	contents							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0	Start byte (0x*a*5, a = device address)							
1	Data Packet Type (0x04)							
2	PacketID bits 7-0							
3	E1	E2	D	S	F	R	I (2 bits)	
4	Packet Tx Latency bits 7-0							
5	Packet Tx Latency bits 15-8							
6	$DeltaV_x$ bits 7-0							
7	$DeltaV_x$ bits 15-8							
8	$DeltaV_y$ bits 7-0							
9	$DeltaV_y$ bits 15-8							
10	$DeltaV_z$ bits 7-0							
11	$DeltaV_z$ bits 15-8							
12	$DeltaTheta_x$ bits 7-0							
13	$DeltaTheta_x$ bits 15-8							
14	$DeltaTheta_y$ bits 7-0							
15	$DeltaTheta_y$ bits 15-8							
16	$DeltaTheta_z$ bits 7-0							
17	$DeltaTheta_z$ bits 15-8							
18	Mag_I bits 7-0							
19	Mag_I bits 15-8							
20	Checksum of bytes 0 to 19							
Note: For information on data items, please refer to section 3.5.								

4 Configuration Register Set

The Configuration Register Set is a 256-byte block of memory containing all of the NavChip's current operating state information, including constants, user-configured parameters, and built-in self-test results. There are multiple ways to read information out of the Configuration Registers:

1) Get Register command reads out any byte(s) in any order.
2) In Streaming Mode, packet types 3 and 4 contain an "S"-bit which cycles through the first 256 bits (32 bytes) of the Configuration Register Set, allowing the receiving program to reconstruct the most important status information once per 256-packet frame.

4.1 Configuration Register Map

Table 13: NavChip Configuration Registers Map

NavChip Register Map					
Register Name	Address (Hex)	Address (Dec)	Type	Default	Description
DEVICE_TYPE	00	0	R	22	Device type
FWVER_MINOR	01	1	R		Firmware minor version
FWVER_MAJOR	02	2	R		Firmware major version
NVRAM_SIZE	03	3	R	16	NVRAM size in 64-byte blocks
SERIAL_BYTE0	04	4	R		Byte 0 (least significant) of serial number
SERIAL_BYTE1	05	5	R		Byte 1 of serial number
SERIAL_BYTE2	06	6	R		Byte 2 (most significant) of serial number
NAVCHIP_TYPE	07	7	R		NavChip type
DEVICE_ADDR	08	8	R/W	0	Device address
RESERVED	09	9	R		Reserved for future use
FRAME_ID_LSB	0A	10	R		Data frame ID (LSB)
FRAME_ID_MSB	0B	11	R		Data frame ID (MSB)
SERIAL_ALPHA1	0C	12	R		First character in serial number
SERIAL_ALPHA2	0D	13	R		Second character in serial number
BAUD_DIV	0E	14	R/W	8	Baud rate divisor
DATA_DIV	0F	15	R/W	5	Data rate divisor
PACKET_TYPE	10	16	R/W	3	Packet type
CONFIG	11	17	R/W	0	User configuration
OP_STATUS	12	18	R		Operational status
RESERVED	13 to 16	19 to 22	R		Reserved for future use
RUNTIME_WARN	17	23	R	0	Runtime warning flags
RESERVED	18	24	R		Reserved for future use
ENVIRO_0	19	25	R		Environmental data register 0 (Temperature)
ENVIRO_1	1A	26	R		Environmental data register 1 (Temperature)
ENVIRO_2	1B	27	R		Environmental data register 2
RESERVED	1C to 23	28 to 35	R		Reserved for future use
QTBIT_RES_0	24	36	R	0	Sensor QBIT/TBIT Results
QTBIT_RES_1	25	37	R	0	Sensor QBIT/TBIT Results
CBIT_RES_0	26	38	R	0	Sensor CBIT Results
CBIT_RES_1	27	39	R	0	Sensor CBIT Results
SYSTEM_STATUS	28	40	R	0	System Status
RUNTIME_STATUS	29	41	R	0	Processor Runtime Status

NavChip Register Map					
COMM_STATUS	2A	42	R	0	Communication Status
RESERVED	2B	43	R		Reserved for future use
BSIGHT_0_0_L	2C	44	R/W	255	Boresight matrix (0, 0), LSB
BSIGHT_0_0_H	2D	45	R/W	127	Boresight matrix (0, 0), MSB
BSIGHT_0_1_L	2E	46	R/W	0	Boresight matrix (0, 1), LSB
BSIGHT_0_1_H	2F	47	R/W	0	Boresight matrix (0, 1), MSB
BSIGHT_0_2_L	30	48	R/W	0	Boresight matrix (0, 2), LSB
BSIGHT_0_2_H	31	49	R/W	0	Boresight matrix (0, 2), MSB
BSIGHT_1_0_L	32	50	R/W	0	Boresight matrix (1, 0), LSB
BSIGHT_1_0_H	33	51	R/W	0	Boresight matrix (1, 0), MSB
BSIGHT_1_1_L	34	52	R/W	255	Boresight matrix (1, 1), LSB
BSIGHT_1_1_H	35	53	R/W	127	Boresight matrix (1, 1), MSB
BSIGHT_1_2_L	36	54	R/W	0	Boresight matrix (1, 2), LSB
BSIGHT_1_2_H	37	55	R/W	0	Boresight matrix (1, 2), MSB
BSIGHT_2_0_L	38	56	R/W	0	Boresight matrix (2, 0), LSB
BSIGHT_2_0_H	39	57	R/W	0	Boresight matrix (2, 0), MSB
BSIGHT_2_1_L	3A	58	R/W	0	Boresight matrix (2, 1), LSB
BSIGHT_2_1_H	3B	59	R/W	0	Boresight matrix (2, 1), MSB
BSIGHT_2_2_L	3C	60	R/W	255	Boresight matrix (2, 2), LSB
BSIGHT_2_2_H	3D	61	R/W	127	Boresight matrix (2, 2), MSB
MAG_HI_0_L	3E	62	R/W	0	Mag hard iron bias X, LSB
MAG_HI_0_H	3F	63	R/W	0	Mag hard iron bias X, MSB
MAG_HI_1_L	40	64	R/W	0	Mag hard iron bias Y, LSB
MAG_HI_1_H	41	65	R/W	0	Mag hard iron bias Y, MSB
MAG_HI_2_L	42	66	R/W	0	Mag hard iron bias Z, LSB
MAG_HI_2_H	43	67	R/W	0	Mag hard iron bias Z, MSB
MAG_SI_0_0_L	44	68	R/W	0	Mag soft iron matrix (0, 0), LSB
MAG_SI_0_0_H	45	69	R/W	0	Mag soft iron matrix (0, 0), MSB
MAG_SI_0_1_L	46	70	R/W	0	Mag soft iron matrix (0, 1), LSB
MAG_SI_0_1_H	47	71	R/W	0	Mag soft iron matrix (0, 1), MSB
MAG_SI_0_2_L	48	72	R/W	0	Mag soft iron matrix (0, 2), LSB
MAG_SI_0_2_H	49	73	R/W	0	Mag soft iron matrix (0, 2), MSB
MAG_SI_1_0_L	4A	74	R/W	0	Mag soft iron matrix (1, 0), LSB
MAG_SI_1_0_H	4B	75	R/W	0	Mag soft iron matrix (1, 0), MSB
MAG_SI_1_1_L	4C	76	R/W	0	Mag soft iron matrix (1, 1), LSB
MAG_SI_1_1_H	4D	77	R/W	0	Mag soft iron matrix (1, 1), MSB

NavChip Register Map					
MAG_SI_1_2_L	4E	78	R/W	0	Mag soft iron matrix (1, 2), LSB
MAG_SI_1_2_H	4F	79	R/W	0	Mag soft iron matrix (1, 2), MSB
MAG_SI_2_0_L	50	80	R/W	0	Mag soft iron matrix (2, 0), LSB
MAG_SI_2_0_H	51	81	R/W	0	Mag soft iron matrix (2, 0), MSB
MAG_SI_2_1_L	52	82	R/W	0	Mag soft iron matrix (2, 1), LSB
MAG_SI_2_1_H	53	83	R/W	0	Mag soft iron matrix (2, 1), MSB
MAG_SI_2_2_L	54	84	R/W	0	Mag soft iron matrix (2, 2), LSB
MAG_SI_2_2_H	55	85	R/W	0	Mag soft iron matrix (2, 2), MSB
CALDATE_BYTE0	56	86	R		Calibration date byte 0 (LSB)
CALDATE_BYTE1	57	87	R		Calibration date byte 1
CALDATE_BYTE2	58	88	R		Calibration date byte 2 (MSB)
DISC_FLAG	59	89	R		Discrete flag byte
CAL_REV_BYTE0	5A	90	R		Calibration revision, byte 0 (LSB)
CAL_REV_BYTE1	5B	91	R		Calibration revision, byte 1 (MSB)
HW_REV	5C	92	R		Hardware revision
RESERVED	5D to 8F	93 to 143	R		Reserved for future use
MAG_NOM_DIP_1	90	144	R/W	0	Magnetometer nominal dip angle (byte 0)
MAG_NOM_DIP_2	91	145	R/W	0	Magnetometer nominal dip angle (byte 1)
MAG_NOM_DIP_3	92	146	R/W	0	Magnetometer nominal dip angle (byte 2)
MAG_NOM_DIP_4	93	147	R/W	0	Magnetometer nominal dip angle (byte 3)
MAG_NOM_MAG_1	94	148	R/W	0	Magnetometer nominal magnitude (byte 0)
MAG_NOM_MAG_2	95	149	R/W	0	Magnetometer nominal magnitude (byte 1)
MAG_NOM_MAG_3	96	150	R/W	0	Magnetometer nominal magnitude (byte 2)
MAG_NOM_MAG_4	97	151	R/W	0	Magnetometer nominal magnitude (byte 3)
RESERVED	98 to 9E	152 to 158	R		Reserved for future use
STREAM_TO	9F	159	R/W	0	Stream timeout in increments of 0.1 seconds
RESERVED	A0 to FE	160 to 254	R		Reserved for future use
SAVE_RESTORE	FF	255	R/W	0	Save/Restore configuration

4.2 Configuration Register Details

Table 14: NavChip Configuration Register Details

Register 0 (0x00) – DEVICE_TYPE								
Description	Device type							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	22							
Bits RW	R							
Bits Name	DEVICE_TYPE							
Details	This register represents the device type (22 for NavChip). It can be tested by user software to help identify and verify that the sensor is in fact a NavChip.							

Register 1 (0x01) – FWVER_MINOR								
Description	Firmware minor version							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	FWVER_MINOR							
Details	The minor version of the firmware; updated when minor changes are made to the firmware.							

Register 2 (0x02) – FWVER_MAJOR								
Description	Firmware major version							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	FWVER_MAJOR							
Details	The major version of the firmware; updated when significant changes are made to the firmware.							

Register 3 (0x03) – NVRAM_SIZE								
Description	NVRAM size in 64-byte blocks							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	16							
Bits RW	R							
Bits Name	NVRAM_SIZE							
Details	This register indicates the size of writeable NVRAM in 64-byte blocks.							

Register 4 (0x04) – SERIAL_BYTE0								
Description	Byte 0 (least significant) of serial number							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	SERIAL_BYTE0							
Details	The serial number is comprised of a 24-bit value (SERIAL_BYTE2, SERIAL_BYTE1, SERIAL_BYTE0, in order of most to lease significant), followed by a two-ASCII-character sequence (SERIAL_ALPHA1, SERIAL_ALPHA2) in that order. These are registers 6, 5, 4, 12 and 13, respectively.							

Register 5 (0x05) – SERIAL_BYTE1								
Description	Byte 1 of serial number							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	SERIAL_BYTE1							
Details	The serial number is comprised of a 24-bit value (SERIAL_BYTE2, SERIAL_BYTE1, SERIAL_BYTE0, in order of most to lease significant), followed by a two-ASCII-character sequence (SERIAL_ALPHA1, SERIAL_ALPHA2) in that order. These are registers 6, 5, 4, 12 and 13, respectively.							

Register 6 (0x06) – SERIAL_BYTE2								
Description	Byte 2 (most significant) of serial number							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	SERIAL_BYTE2							
Details	The serial number is comprised of a 24-bit value (SERIAL_BYTE2, SERIAL_BYTE1, SERIAL_BYTE0, in order of most to lease significant), followed by a two-ASCII-character sequence (SERIAL_ALPHA1, SERIAL_ALPHA2) in that order. These are registers 6, 5, 4, 12 and 13, respectively.							

Register 7 (0x07) – NAVCHIP_TYPE								
Description	NavChip type							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	NAVCHIP_TYPE							
Details	NavChip Type reflects different products with different capabilities (e.g. 0 = 2000°/s ± 8g, 1 = 480°/s, ± 8g, 2 = 2000°/s, ± 16g, 3 = 480°/s, ± 16g).							

Register 8 (0x08) – DEVICE_ADDR								
Description	Device address							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0					0		
Bits RW	R					R/W		
Bits Name	RESERVED					DEV_ADDR		
Details	The NavChip device address. ▪ RESERVED (Bits 7–3) – Reserved for future use ▪ DEV_ADDR (Bits 2–0) – Device address, from 0–7. Used to allow a single transmit line to address multiple NavChips.							

Register 10 (0x0A) – FRAME_ID_LSB								
Description	Data frame ID (LSB)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	FRAME_ID_LSB							
Details	Data frame ID least significant byte. The frame ID starts at 0, and increments every 256 records that have been streamed. At the default rate of 200 Hz, it will wrap around to 0 after 16777216 records have been streamed (23.3 hours).							

Register 11 (0x0B) - FRAME_ID_MSB								
Description	Data frame ID (MSB)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	FRAME_ID_MSB							
Details	Data frame ID most significant byte. The frame ID starts at 0, and increments every 256 records that have been streamed. At the default rate of 200 Hz, it will wrap around to 0 after 16777216 records have been streamed (23.3 hours).							

Register 12 (0x0C) - SERIAL_ALPHA1								
Description	First character in serial number							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	SERIAL_ALPHA1							
Details	The serial number is comprised of a 24-bit value (SERIAL_BYTE2, SERIAL_BYTE1, SERIAL_BYTE0, in order of most to lease significant), followed by a two-ASCII-character sequence (SERIAL_ALPHA1, SERIAL_ALPHA2) in that order. These are registers 6, 5, 4, 12 and 13, respectively.							

Register 13 (0x0D) - SERIAL_ALPHA2								
Description	Second character in serial number							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	SERIAL_ALPHA2							
Details	The serial number is comprised of a 24-bit value (SERIAL_BYTE2, SERIAL_BYTE1, SERIAL_BYTE0, in order of most to lease significant), followed by a two-ASCII-character sequence (SERIAL_ALPHA1, SERIAL_ALPHA2) in that order. These are registers 6, 5, 4, 12 and 13, respectively.							

Register 14 (0x0E) - BAUD_DIV								
Description	Baud rate divisor							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	8							
Bits RW	R/W							
Bits Name	BAUD_DIV							
Details	The baud rate divisor. The sensor will communicate at a baud rate of 921600/BAUD_DIV. Please see table for more information.							

Register 15 (0x0F) - DATA_DIV								
Description	Data rate divisor							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	5							
Bits RW	R/W							
Bits Name	DATA_DIV							
Details	The data rate divisor. The sensor will output data at 1000/DATA_DIV records/second. Please see table for more information.							

Register 16 (0x10) - PACKET_TYPE								
Description	Packet type							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	3							
Bits RW	R/W							
Bits Name	PACKET_TYPE							
Details	This register configures the output packet type (types 3 and 4 are supported).							

Register 17 (0x11) – CONFIG								
Description	User configuration							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Bits RW	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bits Name	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CFG_BORE	CFG_SYNC	CFG_STREAM
Details	This register configures NavChip behavior, including boresight correction, sync, and startup behavior. ▪ RESERVED (Bit 7) – Reserved for future use ▪ RESERVED (Bit 6) – Reserved for future use ▪ RESERVED (Bit 5) – Reserved for future use ▪ RESERVED (Bit 4) – Reserved for future use ▪ RESERVED (Bit 3) – Reserved for future use ▪ CFG_BORE (Bit 2) – Apply user boresight matrix (registers 44–61) to the output data. ▪ CFG_SYNC (Bit 1) – Enables external synchronization as described in the ICD. ▪ CFG_STREAM (Bit 0) – Boot to streaming mode instead of standby mode. Initially defaults to UART communications. Switches to SPI if an SPI command is received.							

Register 18 (0x12) – OP_STATUS								
Description	Operational status							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	
Bits RW	R	R	R	R	R	R	R	
Bits Name	RESERVED	RESERVED	RESERVED	RESERVED	SYNCED	STREAMING	RESERVED	
Details	▪ RESERVED (Bit 7) – Reserved for future use ▪ RESERVED (Bit 6) – Reserved for future use ▪ RESERVED (Bit 5) – Reserved for future use ▪ RESERVED (Bit 4) – Reserved for future use ▪ SYNCED (Bit 3) – Indicates that the NavChip has received/is continuing to receive a valid synchronization signal. ▪ STREAMING (Bit 2) – Indicates that the NavChip is currently streaming data. ▪ RESERVED (Bits 1–0) – Reserved for future use							

Register 23 (0x17) – RUNTIME_WARN								
Description	Runtime warning flags							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Bits RW	R	R	R	R	R	R	R	R
Bits Name	RUNWARN_ SYNCNOW	RUNWARN_ SYNCFAIL	RUNWARN_ INTEG	RUNWARN_ VOLT	RUNWARN_ TEMP	RUNWARN_ MAG	RUNWARN_ ACCEL	RUNWARN_ GYRO
Details	Runtime warning flags indicate that a problem has occurred with the NavChip (not a typical occurrence), or provide status information in the case of the two sync bits. In some cases, such as a failure of gyro or accelerometer data, this may cause the output data to stop updating (this could happen if the NavChip was physically damaged by an extreme impact, for instance). It is recommended that this register be read periodically (i.e. using the S-bits that are output once per frame) to detect any problems soon after they occur. ▪ RUNWARN_SYNCNOW (Bit 7) – Indicates that the sensor is currently synchronizing. ▪ RUNWARN_SYNCFAIL (Bit 6) – Indicates a fault with synchronization (sync is enabled, but the sync signal is missing or invalid). ▪ RUNWARN_INTEG (Bit 5) – Indicates an internal fault with sensor sampling, data from one or more sensors may be invalid. ▪ RUNWARN_VOLT (Bit 4) – Indicates that the supply voltage is out of range. This may have a negative effect on the data calibration or cause other problems with the data. ▪ RUNWARN_TEMP (Bit 3) – Indicates that the temperature has exceeded the calibrated temperature range. Although the sensor will still work, the data calibration will not be optimal. ▪ RUNWARN_MAG (Bit 2) – Indicates that a problem has been detected with the magnetometer data ▪ RUNWARN_ACCEL (Bit 1) – Indicates that a problem has been detected with the accelerometer data. ▪ RUNWARN_GYRO (Bit 0) – Indicates that a problem has been detected with the gyroscope data.							

Register 25 (0x19) – ENVIRO_0								
Description	Environmental data register 0 (Temperature)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	TEMP_BYTE0							
Details	Contains information about the environment the sensor is operating in. ▪ TEMP_BYTE0 (Bits 7–0) – Byte 0 (LSB) of temperature data. Temperature (in Celsius) is 0.05 * ((TEMP_BYTE1 << 8) | TEMP_BYTE0).							

Register 26 (0x1A) – ENVIRO_1								
Description	Environmental data register 1 (Temperature)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies				Varies			
Bits RW	R				R			
Bits Name	RESERVED				TEMP_BYTE1			
Details	Contains information about the environment the sensor is operating in. ▪ RESERVED (Bits 7–4) – Reserved for future use ▪ TEMP_BYTE1 (Bits 3–0) – Byte 1 (upper nibble) of temperature data. Temperature (in Celsius) is 0.05 * ((TEMP_BYTE1 << 8) | TEMP_BYTE0).							

Register 27 (0x1B) – ENVIRO_2								
Description	Environmental data register 2							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	ENVIRO_2							
Details	Currently unused, may contain additional environmental data in a future release.							

Register 36 (0x24) – QTBIT_RES_0								
Description	Sensor QBIT/TBIT Results							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Bits RW	R	R	R	R	R	R	R	R
Bits Name	RESERVED	QTBR_GYRZ	QTBR_GYRY	QTBR_GYRX	QTBR_GYRZ	QTBR_GYRY	QTBR_GYRX	QTBR_TEMP
Details	▪ RESERVED (Bit 7) – Reserved for future use ▪ QTBR_GYRZ (Bit 6) – Z Accel QBIT/TBIT failure ▪ QTBR_GYRY (Bit 5) – Y Accel QBIT/TBIT failure ▪ QTBR_GYRX (Bit 4) – X Accel QBIT/TBIT failure ▪ QTBR_GYRZ (Bit 3) – Z Gyro QBIT/TBIT failure ▪ QTBR_GYRY (Bit 2) – Y Gyro QBIT/TBIT failure ▪ QTBR_GYRX (Bit 1) – X Gyro QBIT/TBIT failure ▪ QTBR_TEMP (Bit 0) – Temperature sensor QBIT/TBIT failure							

Register 37 (0x25) – QTBIT_RES_1								
Description	Sensor QBIT/TBIT Results							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0					0	0	0
Bits RW	R					R	R	R
Bits Name	RESERVED					QTBR_MAGZ	QTBR_MAGY	QTBR_MAGX
Details	▪ RESERVED (Bits 7–3) – Reserved for future use ▪ QTBR_MAGZ (Bit 2) – Z Magnetometer QBIT/TBIT failure ▪ QTBR_MAGY (Bit 1) – Y Magnetometer QBIT/TBIT failure ▪ QTBR_MAGX (Bit 0) – X Magnetometer QBIT/TBIT failure							

Register 38 (0x26) – CBIT_RES_0								
Description	Sensor CBIT Results							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0	0	0	0	0	0	0	0
Bits RW	R	R	R	R	R	R	R	R
Bits Name	RESERVED	CBR_ACCZ	CBR_ACCY	CBR_ACCX	CBR_GYRZ	CBR_GYRY	CBR_GYRX	CBR_TEMP
Details	▪ RESERVED (Bit 7) – Reserved for future use ▪ CBR_ACCZ (Bit 6) – Z Accel CBIT failure ▪ CBR_ACCY (Bit 5) – Y Accel CBIT failure ▪ CBR_ACCX (Bit 4) – X Accel CBIT failure ▪ CBR_GYRZ (Bit 3) – Z Gyro CBIT failure ▪ CBR_GYRY (Bit 2) – Y Gyro CBIT failure ▪ CBR_GYRX (Bit 1) – X Gyro CBIT failure ▪ CBR_TEMP (Bit 0) – Temperature sensor CBIT failure							

Register 39 (0x27) – CBIT_RES_1								
Description	Sensor CBIT Results							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0					0	0	0
Bits RW	R					R	R	R
Bits Name	RESERVED					CBR_MAGZ	CBR_MAGY	CBR_MAGX
Details	▪ RESERVED (Bits 7–3) – Reserved for future use ▪ CBR_MAGZ (Bit 2) – Z Magnetometer CBIT failure ▪ CBR_MAGY (Bit 1) – Y Magnetometer CBIT failure ▪ CBR_MAGX (Bit 0) – X Magnetometer CBIT failure							

Register 40 (0x28) – SYSTEM_STATUS								
Description	System Status							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R							
Bits Name	SYSTEM_STATUS							
Details	System status information (memory and configuration), set during QBIT/TBIT. If this register is not 0, please contact Technical Support for assistance.							

Register 41 (0x29) – RUNTIME_STATUS								
Description	Processor Runtime Status							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R							
Bits Name	RUNTIME_STATUS							
Details	Runtime status information (hardware and program), set during QBIT/TBIT. If this register is not 0, please contact Technical Support for assistance.							

Register 42 (0x2A) – COMM_STATUS								
Description	Communication Status							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0			0	0	0	0	0
Bits RW	R			R	R	R	R	R
Bits Name	RESERVED			CSTAT_BAD_HEAD	CSTAT_BAD_CKSM	CSTAT_BAD_UART	CSTAT_BAD_CMD	CSTAT_BAD_VAL
Details	▪ RESERVED (Bits 7–5) – Reserved for future use ▪ CSTAT_BAD_HEAD (Bit 4) – Invalid command header ▪ CSTAT_BAD_CKSM (Bit 3) – Invalid checksum ▪ CSTAT_BAD_UART (Bit 2) – Invalid UART configuration ▪ CSTAT_BAD_CMD (Bit 1) – Invalid command ▪ CSTAT_BAD_VAL (Bit 0) – Invalid paramter value							

Register 44 (0x2C) – BSIGHT_0_0_L								
Description	Boresight matrix (0, 0), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	255							
Bits RW	R/W							
Bits Name	BSIGHT_0_0_L							
Details	Element (0, 0) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 45 (0x2D) – BSIGHT_0_0_H								
Description	Boresight matrix (0, 0), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	127							
Bits RW	R/W							
Bits Name	BSIGHT_0_0_H							
Details	Element (0, 0) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 46 (0x2E) – BSIGHT_0_1_L								
Description	Boresight matrix (0, 1), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_0_1_L							
Details	Element (0, 1) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 47 (0x2F) – BSIGHT_0_1_H								
Description	Boresight matrix (0, 1), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_0_1_H							
Details	Element (0, 1) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 48 (0x30) – BSIGHT_0_2_L								
Description	Boresight matrix (0, 2), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_0_2_L							
Details	Element (0, 2) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 49 (0x31) – BSIGHT_0_2_H								
Description	Boresight matrix (0, 2), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_0_2_H							
Details	Element (0, 2) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 50 (0x32) – BSIGHT_1_0_L								
Description	Boresight matrix (1, 0), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_1_0_L							
Details	Element (1, 0) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 51 (0x33) – BSIGHT_1_0_H								
Description	Boresight matrix (1, 0), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_1_0_H							
Details	Element (1, 0) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 52 (0x34) – BSIGHT_1_1_L								
Description	Boresight matrix (1, 1), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	255							
Bits RW	R/W							
Bits Name	BSIGHT_1_1_L							
Details	Element (1, 1) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 53 (0x35) – BSIGHT_1_1_H								
Description	Boresight matrix (1, 1), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	127							
Bits RW	R/W							
Bits Name	BSIGHT_1_1_H							
Details	Element (1, 1) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 54 (0x36) – BSIGHT_1_2_L								
Description	Boresight matrix (1, 2), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_1_2_L							
Details	Element (1, 2) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 55 (0x37) – BSIGHT_1_2_H								
Description	Boresight matrix (1, 2), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_1_2_H							
Details	Element (1, 2) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 56 (0x38) – BSIGHT_2_0_L								
Description	Boresight matrix (2, 0), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_2_0_L							
Details	Element (2, 0) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 57 (0x39) – BSIGHT_2_0_H								
Description	Boresight matrix (2, 0), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_2_0_H							
Details	Element (2, 0) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 58 (0x3A) – BSIGHT_2_1_L								
Description	Boresight matrix (2, 1), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_2_1_L							
Details	Element (2, 1) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 59 (0x3B) – BSIGHT_2_1_H								
Description	Boresight matrix (2, 1), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	BSIGHT_2_1_H							
Details	Element (2, 1) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 60 (0x3C) – BSIGHT_2_2_L								
Description	Boresight matrix (2, 2), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	255							
Bits RW	R/W							
Bits Name	BSIGHT_2_2_L							
Details	Element (2, 2) LSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 61 (0x3D) – BSIGHT_2_2_H								
Description	Boresight matrix (2, 2), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	127							
Bits RW	R/W							
Bits Name	BSIGHT_2_2_H							
Details	Element (2, 2) MSB of a boresight rotation matrix. Each element is a 16-bit signed value with a resolution of 1/32768.							

Register 62 (0x3E) – MAG_HI_0_L								
Description	Mag hard iron bias X, LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_HI_0_L							
Details	X magnetometer bias offset in Gauss, LSB. Each element is a 16-bit signed value with a resolution of 1/(2^13), with a range of approximately +4 to -4. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly.							

Register 63 (0x3F) – MAG_HI_0_H								
Description	Mag hard iron bias X, MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_HI_0_H							
Details	X magnetometer bias offset in Gauss, MSB. Each element is a 16-bit signed value with a resolution of 1/(2^13), with a range of approximately +4 to -4. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly.							

Register 64 (0x40) - MAG_HI_1_L								
Description	Mag hard iron bias Y, LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_HI_1_L							
Details	Y magnetometer bias offset in Gauss, LSB. Each element is a 16-bit signed value with a resolution of 1/(2^13), with a range of approximately +4 to -4. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly.							

Register 65 (0x41) - MAG_HI_1_H								
Description	Mag hard iron bias Y, MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_HI_1_H							
Details	Y magnetometer bias offset in Gauss, MSB. Each element is a 16-bit signed value with a resolution of 1/(2^13), with a range of approximately +4 to -4. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly.							

Register 66 (0x42) - MAG_HI_2_L								
Description	Mag hard iron bias Z, LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_HI_2_L							
Details	Z magnetometer bias offset in Gauss, LSB. Each element is a 16-bit signed value with a resolution of 1/(2^13), with a range of approximately +4 to -4. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly.							

Register 67 (0x43) - MAG_HI_2_H								
Description	Mag hard iron bias Z, MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_HI_2_H							
Details	Z magnetometer bias offset in Gauss, MSB. Each element is a 16-bit signed value with a resolution of 1/(2^13), with a range of approximately +4 to -4. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly.							

Register 68 (0x44) - MAG_SI_0_0_L								
Description	Mag soft iron matrix (0, 0), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_0_0_L							
Details	Element (0, 0) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly.							

Register 69 (0x45) - MAG_SI_0_0_H								
Description	Mag soft iron matrix (0, 0), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_0_0_H							
Details	Element (0, 0) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 70 (0x46) - MAG_SI_0_1_L								
Description	Mag soft iron matrix (0, 1), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_0_1_L							
Details	Element (0, 1) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 71 (0x47) - MAG_SI_0_1_H								
Description	Mag soft iron matrix (0, 1), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_0_1_H							
Details	Element (0, 1) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 72 (0x48) - MAG_SI_0_2_L								
Description	Mag soft iron matrix (0, 2), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_0_2_L							
Details	Element (0, 2) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 73 (0x49) - MAG_SI_0_2_H								
Description	Mag soft iron matrix (0, 2), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_0_2_H							
Details	Element (0, 2) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 74 (0x4A) - MAG_SI_1_0_L								
Description	Mag soft iron matrix (1, 0), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_1_0_L							
Details	Element (1, 0) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 75 (0x4B) - MAG_SI_1_0_H								
Description	Mag soft iron matrix (1, 0), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_1_0_H							
Details	Element (1, 0) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 76 (0x4C) - MAG_SI_1_1_L								
Description	Mag soft iron matrix (1, 1), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_1_1_L							
Details	Element (1, 1) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 77 (0x4D) - MAG_SI_1_1_H								
Description	Mag soft iron matrix (1, 1), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_1_1_H							
Details	Element (1, 1) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 78 (0x4E) - MAG_SI_1_2_L								
Description	Mag soft iron matrix (1, 2), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_1_2_L							
Details	Element (1, 2) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 79 (0x4F) - MAG_SI_1_2_H								
Description	Mag soft iron matrix (1, 2), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_1_2_H							
Details	Element (1, 2) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 80 (0x50) - MAG_SI_2_0_L								
Description	Mag soft iron matrix (2, 0), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_2_0_L							
Details	Element (2, 0) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 81 (0x51) - MAG_SI_2_0_H								
Description	Mag soft iron matrix (2, 0), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_2_0_H							
Details	Element (2, 0) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 82 (0x52) - MAG_SI_2_1_L								
Description	Mag soft iron matrix (2, 1), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_2_1_L							
Details	Element (2, 1) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 83 (0x53) - MAG_SI_2_1_H								
Description	Mag soft iron matrix (2, 1), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_2_1_H							
Details	Element (2, 1) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 84 (0x54) - MAG_SI_2_2_L								
Description	Mag soft iron matrix (2, 2), LSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_2_2_L							
Details	Element (2, 2) LSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 85 (0x55) - MAG_SI_2_2_H								
Description	Mag soft iron matrix (2, 2), MSB							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_SI_2_2_H							
Details	Element (2, 2) MSB of the magnetometer soft iron matrix. Each element is a 16-bit signed value with a resolution of 1/(2^12), with a range of approximately +8.0 to -8.0. Currently set/used by the DLL only (when set to a value other than 0, on NavChips with magnetometers), and not applied by the NavChip, though later firmware versions may apply it directly..							

Register 86 (0x56) - CALDATE_BYTE0								
Description	Calibration date byte 0 (LSB)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	CALDATE_BYTE0							
Details	Calibration date in "2YYYMMDD" format, and values are stored in MMDDYYY format. Value is a 24-bit unsigned integer, ((CALDATE_BYTE2 << 16) | (CALDATE_BYTE1 << 8) | (CALDATE_BYTE0)). For example, 2015-03-22 would be stored as the integer 322015 (or 0x04E9DF), which would mean CALDATE_BYTE0 through CALDATE_BYTE2 would be 223 (0xDF), 233 (0xE9), 4 (0x04), respectively; (4<<16) | (233<<8) | (223) = 322015.							

Register 87 (0x57) - CALDATE_BYTE1								
Description	Calibration date byte 1							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	CALDATE_BYTE1							
Details	Calibration date in "2YYYMMDD" format, and values are stored in MMDDYYY format. Value is a 24-bit unsigned integer, ((CALDATE_BYTE2 << 16) | (CALDATE_BYTE1 << 8) | (CALDATE_BYTE0)). For example, 2015-03-22 would be stored as the integer 322015 (or 0x04E9DF), which would mean CALDATE_BYTE0 through CALDATE_BYTE2 would be 223 (0xDF), 233 (0xE9), 4 (0x04), respectively; (4<<16) | (233<<8) | (223) = 322015.							

Register 88 (0x58) – CALDATE_BYTE2								
Description	Calibration date byte 2 (MSB)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	CALDATE_BYTE2							
Details	Calibration date in "2YYYMMDD" format, and values are stored in MMDDYYY format. Value is a 24-bit unsigned integer, ((CALDATE_BYTE2 << 16) | (CALDATE_BYTE1 << 8) | (CALDATE_BYTE0)). For example, 2015-03-22 would be stored as the integer 322015 (or 0x04E9DF), which would mean CALDATE_BYTE0 through CALDATE_BYTE2 would be 223 (0xDF), 233 (0xE9), 4 (0x04), respectively; (4<<16) | (233<<8) | (223) = 322015.							

Register 89 (0x59) – DISC_FLAG								
Description	Discrete flag byte							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies	Varies	Varies	Varies	Varies	Varies	Varies	
Bits RW	R	R	R	R	R	R	R	
Bits Name	DFB_E1	DFB_E2	DFB_D	DFB_S	DFB_F	DFB_R	DFB_I	
Details	▪ DFB_E1 (Bit 7) – The E1 flag notifies that the output sync pulse has been sent out in the current output integration period. ▪ DFB_E2 (Bit 6) – The E2 flag can be used to notify events (currently reserved). ▪ DFB_D (Bit 5) – Reserved for future use ▪ DFB_S (Bit 4) – The S flag represents the value of the nth bit of the first 32 Configuration Registers (256 bits), where n is determined by PacketID. This allows streaming of the first 32 configuration registers (0–31) every frame. Bits are sent from least to most significant, i.e. packet ID 0 will be bit 0 of register 0, packet ID 10 will be bit 1 of register 1, etc. In general, the bit sent is bit (PACKET_ID % 8) of register floor(PACKET_ID/8). At 200 Hz, this allows registers 0–31 to be reconstructed every 1.28 seconds, if no data packets are missed during that time. ▪ DFB_F (Bit 3) – Fault bit, set if there are any runtime warnings; additional information on the fault will be available in register 23 (RUNTIME_WARN). ▪ DFB_R (Bit 2) – Reserved for future use ▪ DFB_I (Bits 1–0) – The index of MagI (0 = no mag data valid, 1 = X mag, 2 = Y mag, 3 = Z mag).							

Register 90 (0x5A) - CAL_REV_BYTE0								
Description	Calibration revision, byte 0 (LSB)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	CAL_REV_BYTE0							
Details	The NavChip calibration revision is a 16-bit unsigned value that represents version of the calibration (this version changes if the calibration methods change, such as if a new calibration technique is introduced). Certain firmware versions upgrades may require recalibration in order to work properly with a NavChip.							

Register 91 (0x5B) - CAL_REV_BYTE1								
Description	Calibration revision, byte 1 (MSB)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	CAL_REV_BYTE1							
Details	The NavChip calibration revision is a 16-bit unsigned value that represents version of the calibration (this version changes if the calibration methods change, such as if a new calibration technique is introduced). Certain firmware versions upgrades may require recalibration in order to work properly with a NavChip.							

Register 92 (0x5C) - HW_REV								
Description	Hardware revision							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	Varies							
Bits RW	R							
Bits Name	HW_REV							
Details	Indicates the hardware revision of the NavChip; changes when internal components of the NavChip change; firmware is specific to hardware revisions (i.e. it is not possible to use a firmware intended for a hardware revision 'A' NavChip in a hardware revision 'B' NavChip, and vice versa). The revision is numeric, but is referred to as the corresponding ASCII character in some software (e.g. revision 71 is the same as revision 'G').							

Register 144 (0x90) - MAG_NOM_DIP_1								
Description	Magnetometer nominal dip angle (byte 0)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_NOM_DIP_1							
Details	IEE-754 float (byte 1) of magnetometer nominal dip angle. Written/used by the InterSense DLL via ISDemo or other software. Used to help the DLL partially/completely disable use of the compass when near sources of magnetic interference. Does not affect NavChip behavior when not used with the DLL.							

Register 145 (0x91) - MAG_NOM_DIP_2								
Description	Magnetometer nominal dip angle (byte 1)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_NOM_DIP_2							
Details	IEE-754 float (byte 2) of magnetometer nominal dip angle. Written/used by the InterSense DLL via ISDemo or other software. Used to help the DLL partially/completely disable use of the compass when near sources of magnetic interference. Does not affect NavChip behavior when not used with the DLL.							

Register 146 (0x92) - MAG_NOM_DIP_3								
Description	Magnetometer nominal dip angle (byte 2)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_NOM_DIP_3							
Details	IEE-754 float (byte 3) of magnetometer nominal dip angle. Written/used by the InterSense DLL via ISDemo or other software. Used to help the DLL partially/completely disable use of the compass when near sources of magnetic interference. Does not affect NavChip behavior when not used with the DLL.							

Register 147 (0x93) - MAG_NOM_DIP_4								
Description	Magnetometer nominal dip angle (byte 3)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_NOM_DIP_4							
Details	IEE-754 float (byte 4) of magnetometer nominal dip angle. Written/used by the InterSense DLL via ISDemo or other software. Used to help the DLL partially/completely disable use of the compass when near sources of magnetic interference. Does not affect NavChip behavior when not used with the DLL.							

Register 148 (0x94) - MAG_NOM_MAG_1								
Description	Magnetometer nominal magnitude (byte 0)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_NOM_MAG_1							
Details	IEE-754 float (byte 1) of magnetometer nominal magnitude (in Gauss). Written/used by the InterSense DLL via ISDemo or other software. Used to help the DLL partially/completely disable use of the compass when near sources of magnetic interference. Does not affect NavChip behavior when not used with the DLL.							

Register 149 (0x95) - MAG_NOM_MAG_2								
Description	Magnetometer nominal magnitude (byte 1)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_NOM_MAG_2							
Details	IEE-754 float (byte 2) of magnetometer nominal magnitude (in Gauss). Written/used by the InterSense DLL via ISDemo or other software. Used to help the DLL partially/completely disable use of the compass when near sources of magnetic interference. Does not affect NavChip behavior when not used with the DLL.							

Register 150 (0x96) - MAG_NOM_MAG_3								
Description	Magnetometer nominal magnitude (byte 2)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_NOM_MAG_3							
Details	IEE-754 float (byte 3) of magnetometer nominal magnitude (in Gauss). Written/used by the InterSense DLL via ISDemo or other software. Used to help the DLL partially/completely disable use of the compass when near sources of magnetic interference. Does not affect NavChip behavior when not used with the DLL.							

Register 151 (0x97) - MAG_NOM_MAG_4								
Description	Magnetometer nominal magnitude (byte 3)							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	MAG_NOM_MAG_4							
Details	IEE-754 float (byte 4) of magnetometer nominal magnitude (in Gauss). Written/used by the InterSense DLL via ISDemo or other software. Used to help the DLL partially/completely disable use of the compass when near sources of magnetic interference. Does not affect NavChip behavior when not used with the DLL.							

Register 159 (0x9F) - STREAM_TO								
Description	Stream timeout in increments of 0.1 seconds							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	STREAM_TO							
Details	Activates the stream timeout feature. When non-zero, streaming data will only be streamed for the register value times 0.1 seconds (i.e. setting the register to 10 will automatically stop the streaming of data after 1.0 seconds). To continue streaming data, the "Start Streaming" command must be sent before the timeout occurs. The register value is NOT saved when saving register values to flash, and is cleared automatically once it reaches zero. Note that as long as communication with the NavChip is reliable, streaming can also be stopped by sending the NavChip the "Ping/Stop Streaming" command; therefore most users should not need to set this register.							

Register 255 (0xFF) – SAVE_RESTORE								
Description	Save/Restore configuration							
Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default	0							
Bits RW	R/W							
Bits Name	SAVE_RESTORE							
Details	Saves configuration registers, or restores configuration registers to default values. Setting this register to 0 saves the registers to flash memory (persists after a power cycle). Setting it to 1 restores all registers to default values (note that this will change the baud rate if a baud rate other than 115200 baud is in use). Also, note that restoring the registers to default values will NOT write the new defaults to flash memory, unless a 0 is written to the register afterwards to save the new default register values.							