



ALPHA & OMEGA
SEMICONDUCTOR

AOC2804B

20V Common-Drain Dual N-Channel AlphaMOS

General Description

- Trench Power AlphaMOS (α MOS LV) technology
- Low $R_{SS(ON)}$
- Fully protected AlphaDFN package
- With ESD protection to improve battery performance and safety
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

Applications

- Battery protection switch
- Mobile device battery charging and discharging

Product Summary

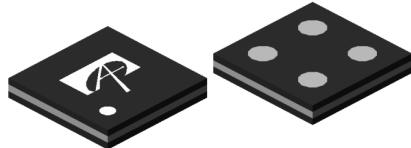
| | |
|----------------------------------|----------------|
| V_{SS} | 20V |
| $R_{SS(ON)}$ (at $V_{GS}=4.5V$) | < 34m Ω |
| $R_{SS(ON)}$ (at $V_{GS}=4.0V$) | < 38m Ω |
| $R_{SS(ON)}$ (at $V_{GS}=3.7V$) | < 40m Ω |
| $R_{SS(ON)}$ (at $V_{GS}=3.1V$) | < 45m Ω |
| $R_{SS(ON)}$ (at $V_{GS}=2.5V$) | < 56m Ω |

Typical ESD protection

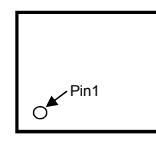
HBM Class 3A



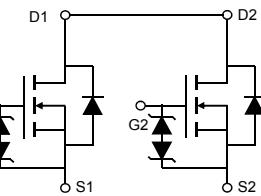
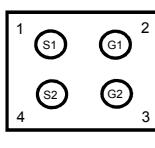
AlphaDFN 1.5x1.5_4
Top View Bottom View



Top View



Bottom View



| Orderable Part Number | Package Type | Form | Minimum Order Quantity |
|-----------------------|--------------------|-------------|------------------------|
| AOC2804B | AlphaDFN 1.5x1.5_4 | Tape & Reel | 3000 |

Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

| Parameter | Symbol | Rating | Units |
|--|--------------------------|------------|-------|
| Source-Source Voltage | V_{SS} | 20 | V |
| Gate-Source Voltage | V_{GS} | ± 12 | V |
| Source Current(DC) ^{Note1} | I_S $T_A=25^\circ C$ | 6 | A |
| Source Current(Pulse) ^{Note2} | I_{SM} | 60 | |
| Power Dissipation ^{Note1} | P_D $T_A=25^\circ C$ | 1.3 | W |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | °C |

Thermal Characteristics

| Parameter | Symbol | Typ | Units |
|--|-----------------|-----|-------|
| Maximum Junction-to-Ambient $t \leq 10s$ | $R_{\theta JA}$ | 85 | °C/W |
| Maximum Junction-to-Ambient Steady-State | | 96 | °C/W |

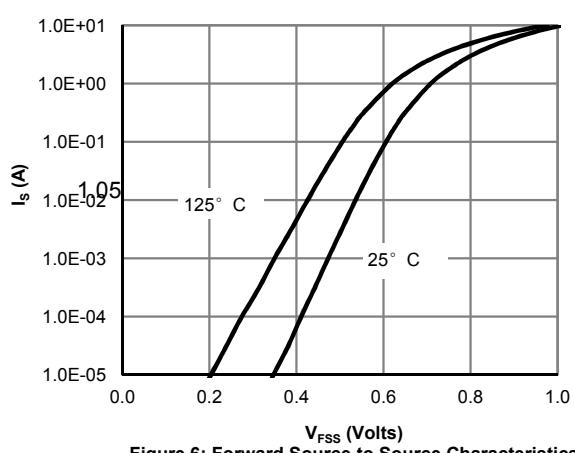
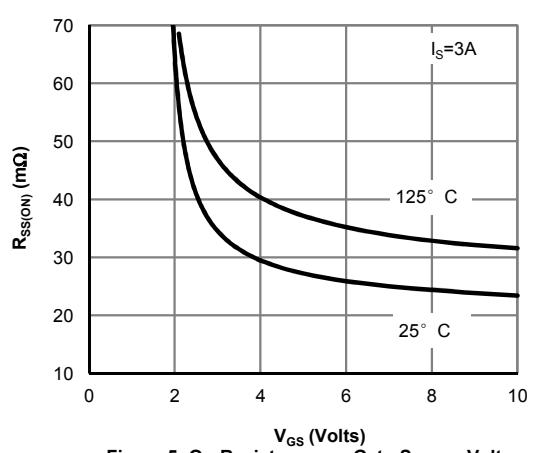
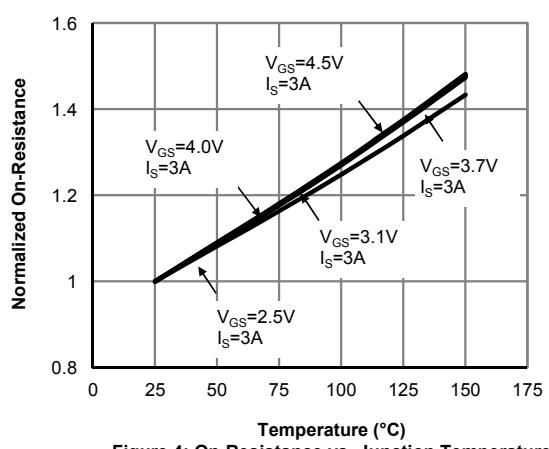
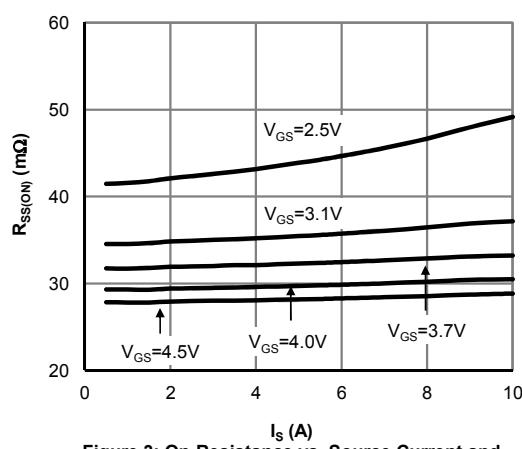
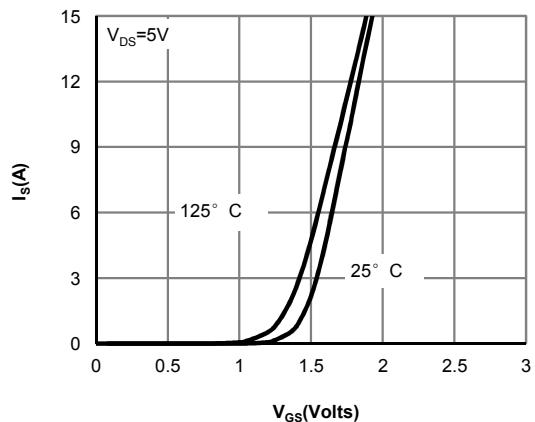
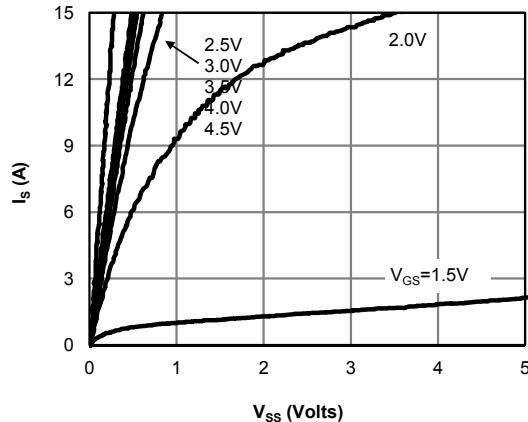
Note 1. I_S rated value is based on bare silicon. Mounted on 70mmx70mm FR-4 board.

Note 2. PW <10 μ s pulses, duty cycle 1% max.

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|-----------------------------|---------------------------------------|---|------------------------|------|----------|------------------|------------------|
| STATIC PARAMETERS | | | | | | | |
| BV_{SSS} | Source-Source Breakdown Voltage | $I_S=250\mu\text{A}, V_{GS}=0\text{V}$ | Test Circuit 6 | 20 | | V | |
| I_{SSS} | Zero Gate Voltage Source Current | $V_{SS}=20\text{V}, V_{GS}=0\text{V}$ | Test Circuit 1 | | 1 | μA | |
| | | | $T_J=55^\circ\text{C}$ | | 5 | | |
| I_{GSS} | Gate leakage current | $V_{SS}=0\text{V}, V_{GS}=\pm 10\text{V}$ | Test Circuit 2 | | ± 10 | μA | |
| $V_{GS(\text{th})}$ | Gate Threshold Voltage | $V_{SS}=V_{GS}, I_S=250\mu\text{A}$ | Test Circuit 3 | 0.5 | 0.9 | 1.3 | V |
| $R_{SS(\text{ON})}$ | Static Source to Source On-Resistance | $V_{GS}=4.5\text{V}, I_S=3\text{A}$ | Test Circuit 4 | 20 | 28 | 34 | $\text{m}\Omega$ |
| | | $T_J=125^\circ\text{C}$ | | 27 | 38.5 | 47 | |
| | | $V_{GS}=4.0\text{V}, I_S=3\text{A}$ | Test Circuit 4 | 22 | 30.5 | 38 | $\text{m}\Omega$ |
| | | $V_{GS}=3.7\text{V}, I_S=3\text{A}$ | Test Circuit 4 | 23 | 32 | 40 | $\text{m}\Omega$ |
| | | $V_{GS}=3.1\text{V}, I_S=3\text{A}$ | Test Circuit 4 | 25 | 35 | 45 | $\text{m}\Omega$ |
| g_{FS} | Forward Transconductance | $V_{SS}=5\text{V}, I_S=3\text{A}$ | Test Circuit 3 | | 20 | | S |
| | | | | | | | |
| V_{FSS} | Forward Source to Source Voltage | $I_S=1\text{A}, V_{GS}=0\text{V}$ | Test Circuit 5 | | 0.72 | 1 | V |
| DYNAMIC PARAMETERS | | | | | | | |
| R_g | Gate resistance | $f=1\text{MHz}$ | | | 2 | $\text{k}\Omega$ | |
| SWITCHING PARAMETERS | | | | | | | |
| Q_g | Total Gate Charge | $V_{G1S1}=4.5\text{V}, V_{SS}=10\text{V}, I_S=3\text{A}$ | | 9.5 | | nC | |
| $t_{D(\text{on})}$ | Turn-On DelayTime | $V_{G1S1}=4.5\text{V}, V_{SS}=10\text{V}, R_L=3.3\Omega,$ $R_{\text{GEN}}=3\Omega$ | Test Circuit 8 | 0.85 | | μs | |
| t_r | Turn-On Rise Time | | | 2.2 | | μs | |
| $t_{D(\text{off})}$ | Turn-Off DelayTime | | | 2.0 | | μs | |
| t_f | Turn-Off Fall Time | | | 4.3 | | μs | |

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


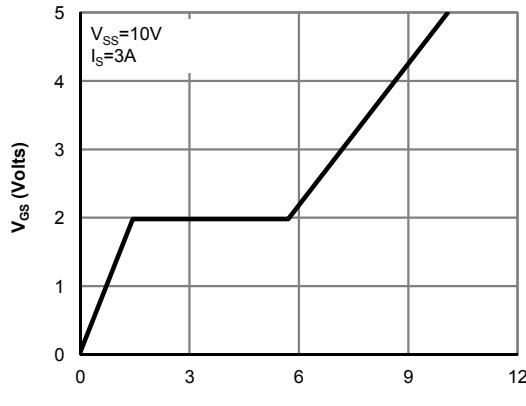
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


Figure 7: Gate-Charge Characteristics

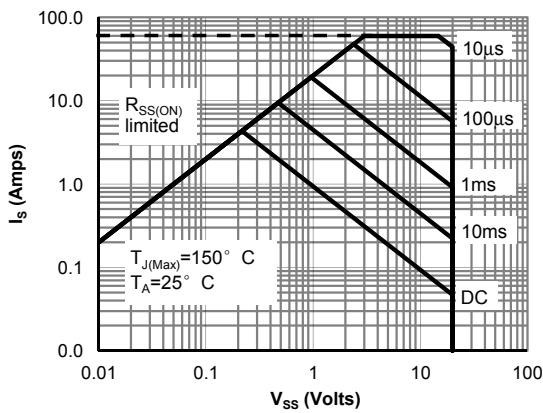
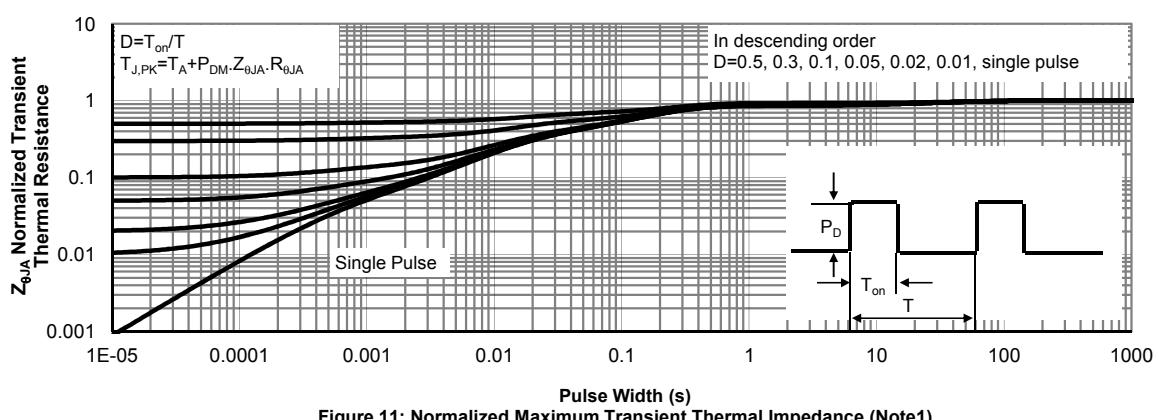
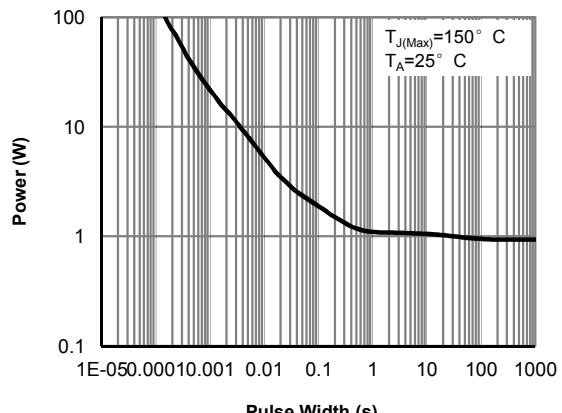
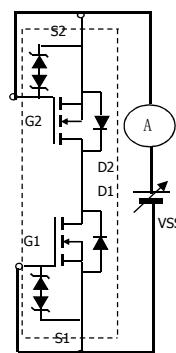


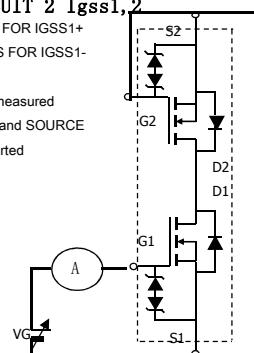
Figure 9: Maximum Forward Biased Safe Operating Area (Note1)



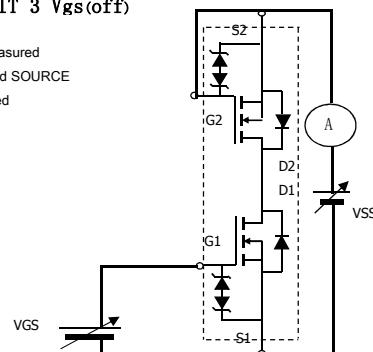
TEST CIRCUIT 1 Isss
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



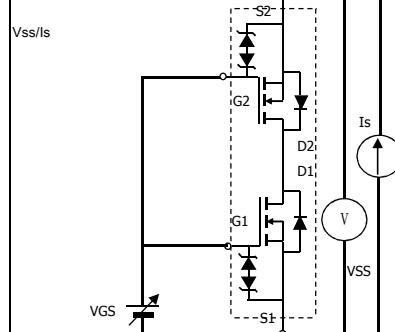
TEST CIRCUIT 2 Igss1,2
POSITIVE VGS FOR IGSS1+
NEGATIVE VGS FOR IGSS1-



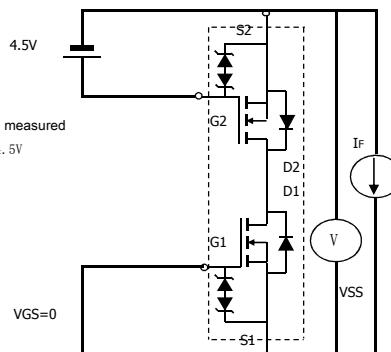
TEST CIRCUIT 3 Vgs(off)
When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



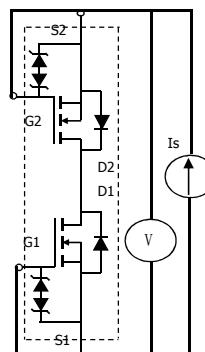
TEST CIRCUIT 4 Rss(on)



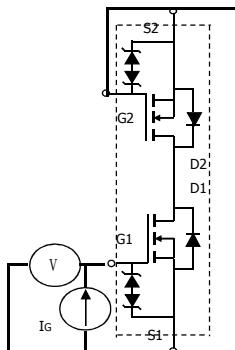
TEST CIRCUIT 5 VF(ss)1,2
4.5V
When FET1 measured
FET2 VGS=4.5V
VGS=0



TEST CIRCUIT 6 BVdss
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-



TEST CIRCUIT 7 BVgs01,2
POSITIVE VSS FOR ISSS+
NEGATIVE VSS FOR ISSS-
When FET1 is measured
between GATE and SOURCE
of FET2 are shorted



TEST CIRCUIT 8
Switching time

