TJA1102

100BASE-T1 dual/single PHY for automotive Ethernet

Rev. 1 — 1 November 2017 Product short data sheet

1. General description

The TJA1102 is a 100BASE-T1 compliant dual-port Ethernet PHY optimized for automotive use cases such as gateways, IP camera links, driver assistance systems and back-bone networks. The device provides 100 Mbit/s transmit and receive capability over two unshielded twisted-pair cables, supporting a cable length of up to at least 15 m. The TJA1102 has been designed for automotive robustness, while minimizing power consumption and system costs. For added flexibility, a single PHY version is available (TJA1102S) in which one of the PHYs is disabled.

For the full data sheet and application hints, please register with DocStore at https://www.docstore.nxp.com.

2. Features and benefits

2.1 General

- Dual-port 100BASE-T1 PHY
- Single-port operation possible
- MII- and RMII-compliant interfaces to the bus
- HVQFN 56-pin package (8 × 8 mm)

2.2 Optimized for automotive use cases

- Transmitter optimized for capacitive coupling to unshielded twisted-pair cable
- Adaptive receive equalizer optimized for automotive cable length of up to at least 15 m
- Enhanced integrated PAM-3 pulse shaping for low RF emissions
- EMC-optimized output driver strength for MII and RMII
- MDI pins protected against transients in automotive environment
- MDI pins do not need external filtering or ESD protection
- Automotive-grade temperature range from −40 °C to +125 °C
- Automotive product qualification in accordance with AEC-Q100

2.3 Low-power mode

- Dedicated PHY enable/disable input pin to minimize power consumption
- Inhibit output for voltage regulator control
- OPEN Alliance-compliant wake-up concept (global wake-up support)
  - Robust remote wake-up detection via bus lines
  - Wake-up forwarding on PHY level
- OPEN Alliance-compliant sleep concept

- Local wake-up pin
- Wake-up via SMI-access

2.4 Diagnosis

- Real-time monitoring of link stability and transmitted data quality
- Diagnosis of cable errors (shorts and opens)
- Gap-free supply undervoltage detection with fail-silent behavior
- Internal, external and remote loopback modes for diagnosis

2.5 Miscellaneous

- Internal reverse MII mode for repeater operation
- On-chip regulators to provide 3.3 V single-supply operation
- Supports optional 1.8 V external supply for digital core
- On-chip termination resistors for the differential cable pair
- Jumbo frame support up to 16 kB

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1102HN[1]	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-13
TJA1102SHN[2]			

[1] Dual PHY.

[2] Single PHY.

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4. Block diagram

A block diagram of the TJA1102 is shown in Figure 1. The 100BASE-T1 sections contain the functional blocks specified in the 100BASE-T1 standard that make up the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) layer for both the transmit and receive signal paths. The MII/RMII interface (including the Serial Management Interface (SMI)) conforms to IEEE802.3 clause 22.

Additional blocks are defined for mode control, register configuration, interrupt control, system configuration, reset control, local wake-up, remote wake-up, undervoltage detection and configuration control. A number of power-supply-related functional blocks are defined: an internal 1.8 V regulator for the digital core, a Very Low Power (VLP) supply for Sleep mode, the reset circuit, supply monitoring and inhibit control.

The clock signals needed for the operation of the PHY are generated in the PLL block, derived from an external crystal or an oscillator input signal.

Pin strapping allows a number of default PHY settings (e.g. Master or Slave configuration) to be hardware-configured at power-up.

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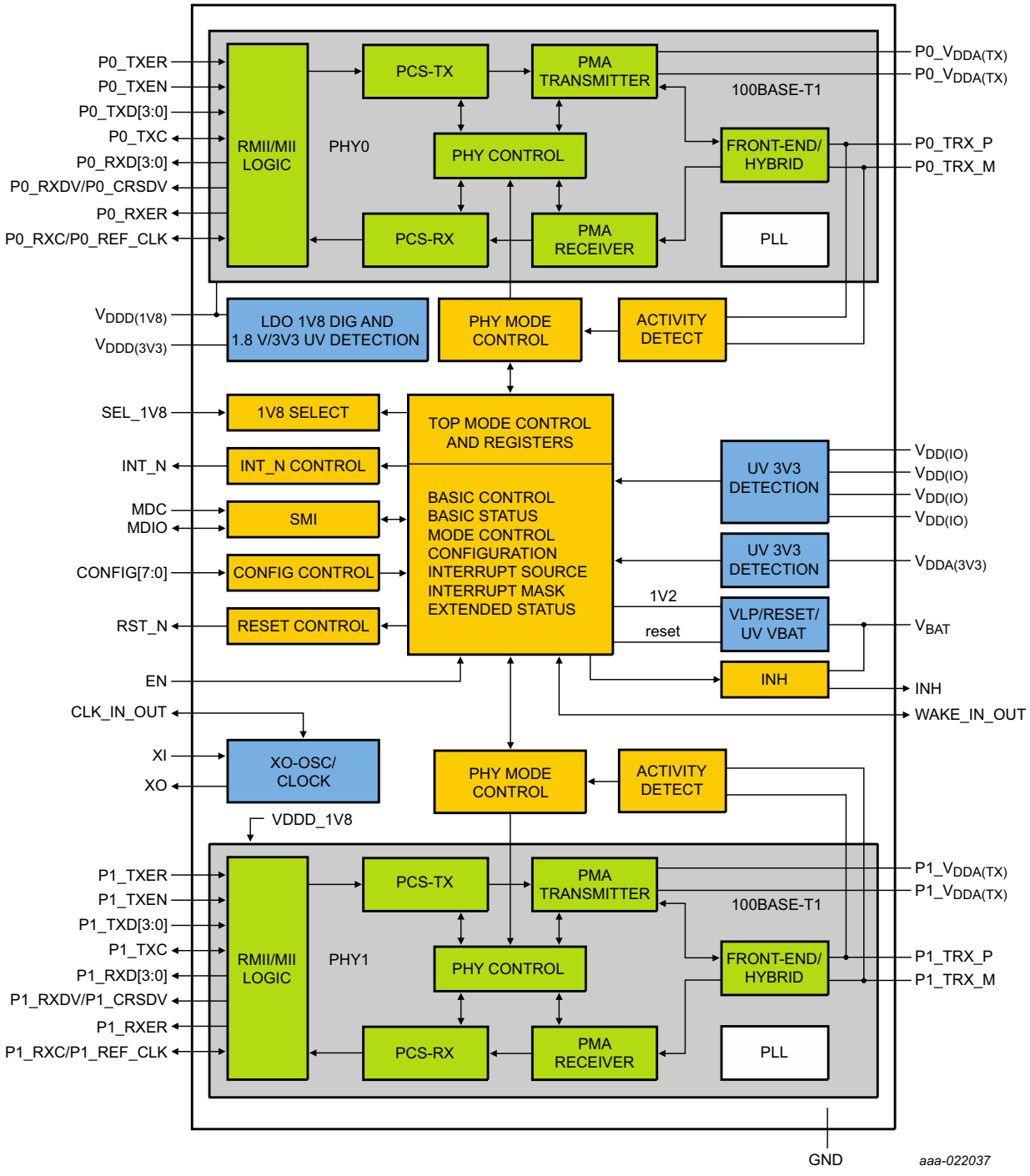

Fig 1. Block diagram (PHY1 is disabled in TJA1102S)

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5. Functional description

5.1 System configuration

The TJA1102 comprises two 100BASE-T1 compliant Ethernet PHYs, with 100 Mbit/s transmit and receive capability over a single unshielded twisted-pair cable. The TJA1102 supports a cable length of up to at least 15 m, with a bit error rate of 1E-10 or less. It is optimized for capacitive signal coupling to the twisted-pair lines. A common-mode choke is typically inserted into the signal path to comply with automotive EMC requirements.

The TJA1102 is designed to provide a cost-optimized system solution for automotive Ethernet links. It communicates with the Media Access Control (MAC) unit via the MII or RMII interface. In combination with other devices, it offers a highly flexible 4-port switch solution, with two TJA1102 Dual PHYs providing the 100BASE-T1 physical layer ports.

The TJA1102 can operate with a crystal or an external clock. The clock can be forwarded to other PHYs (in the application diagram in Figure 2, the clock of one TJA1102 is used as reference for a second TJA1102). The clocking and power supply schemes are independent of each other.

Control and status information is exchanged with the host controller via the SMI interface. The INH output can be used to switch off the external regulator when all ports are in Sleep mode.

Note that the Dual PHY can be configured to operate as a single PHY via pin strapping or the SMI. Alternatively, a TJA1102S could be used when only a single PHY is needed.

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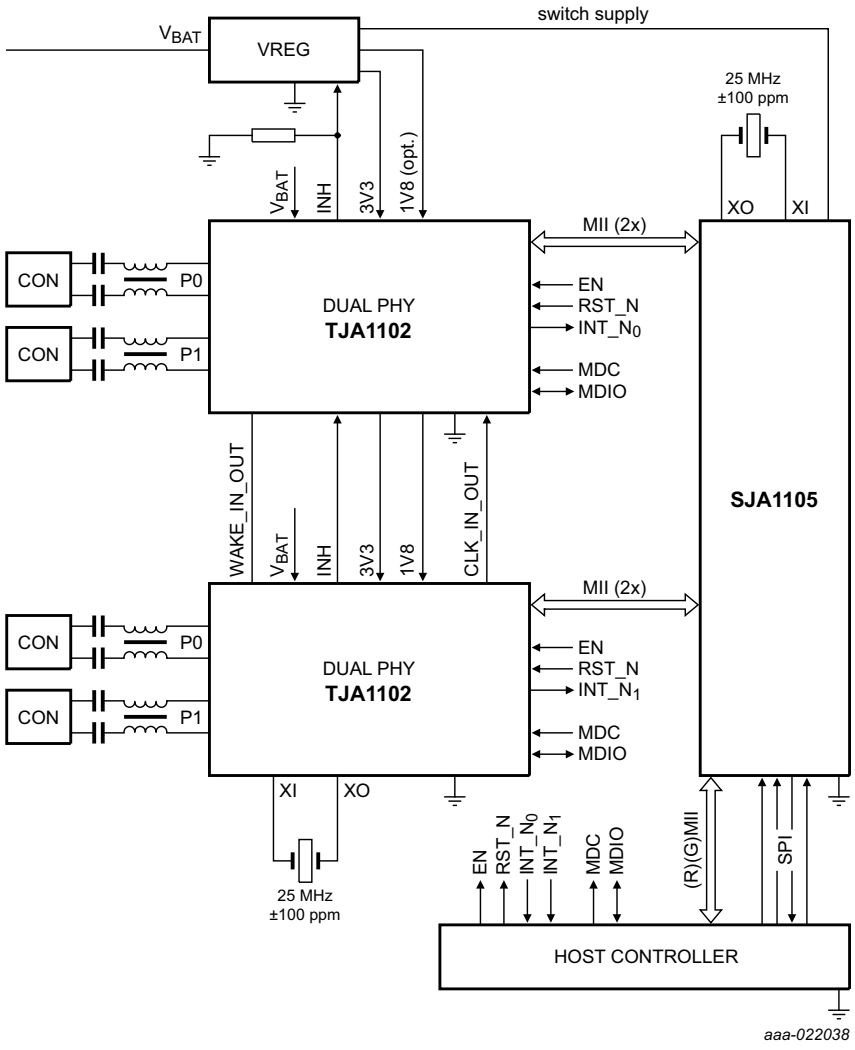
5.1.1 Clocking scheme with MII and clock provided by the switch and one of the TJA1102 devices



One of the TJA1102 devices could be replaced by a TJA1102S if only three PHYs are needed.

Fig 2. Typical TJA1102 MII switch application with SJA1105

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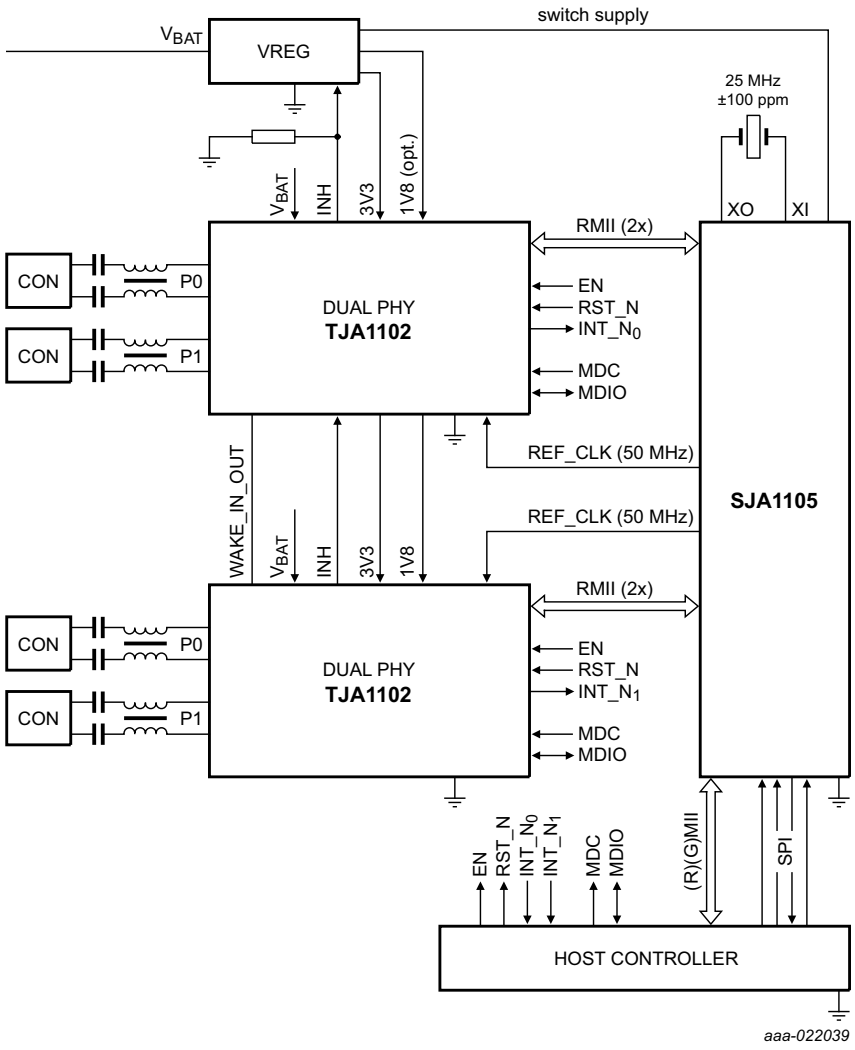
5.1.2 Clocking scheme with RMII and clock provided by the switch



One of the TJA1102 devices could be replaced by a TJA1102S if only three PHYs are needed.

Fig 3. Typical RMII switch application with SJA1105 (XTAL at SJA1105)

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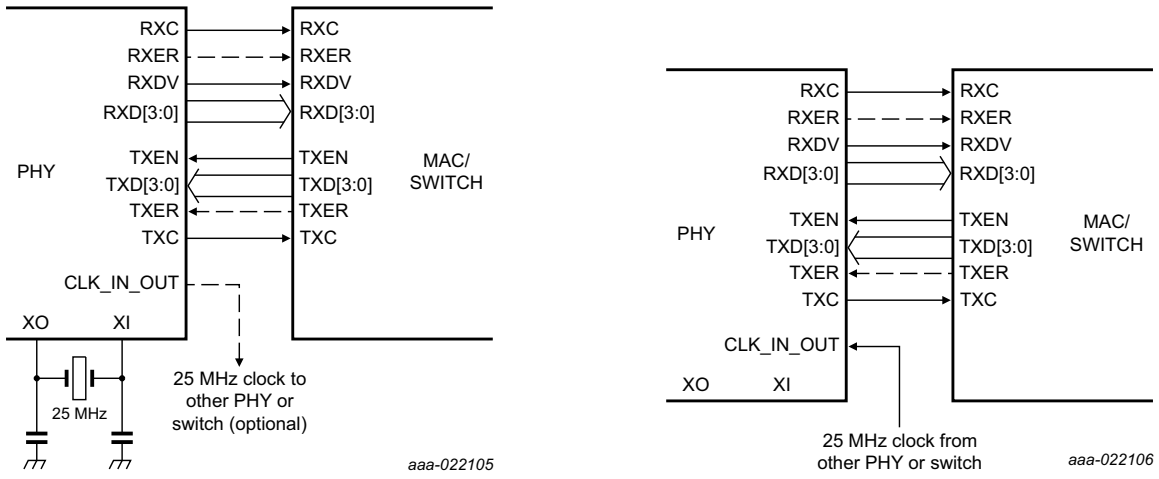
5.2 MII and RMII

The TJA1102 supports a number of MII modes that can be selected via pin strapping or the SMI. The PHYs should be configured to operate in the same mode, with common clocking. The following modes are supported:

- MII
- RMII (25 MHz XTAL or external 50 MHz via REF_CLK)
- Reverse MII (connected externally or internally to the second PHY)

5.2.1 MII

The connections between the PHY and the MAC are shown in more detail in Figure 4. Data is exchanged via 4-bit wide data nibbles on TXD[3:0] and RXD[3:0]. Transmit and receive data is synchronized with the transmit (TXC) and receive (RXC) clocks. Both clock signals are provided by the PHY and are typically derived from an external clock or crystal running at a nominal frequency of 25 MHz (±100 ppm). Normal data transmission is initiated with a HIGH level on TXEN, while a HIGH level on RXDV indicates normal data reception.



a. Using external XTAL showing optional 25 MHz clock output

b. Using external reference clock

Fig 4. MII signaling

5.2.2 RMII

5.2.2.1 Signaling and encoding

RMII data is exchanged via 2-bit wide data nibbles on TXD[1:0] and RXD[1:0], as illustrated in Figure 5. To achieve the same data rate as MII, the interface is clocked at a nominal frequency of 50 MHz. A single clock signal, REF_CLK, is provided for both transmit and received data. This clock signal is provided by the PHY and is typically derived from an external 25 MHz (±100 ppm) crystal (see Figure 5 (a)). Alternatively, a 50 MHz clock signal (±50 ppm) generated by an external oscillator can be connected to pin REF_CLK (see Figure 5 (b)). A third option is to connect a 25 MHz (±100 ppm) clock signal generated by another PHY or switch to pin CLK_IN_OUT (see Figure 5 (c)).

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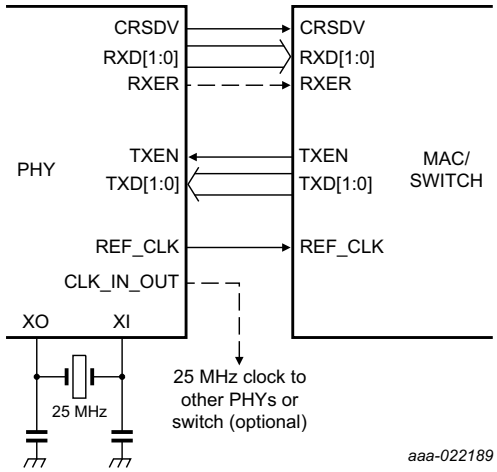
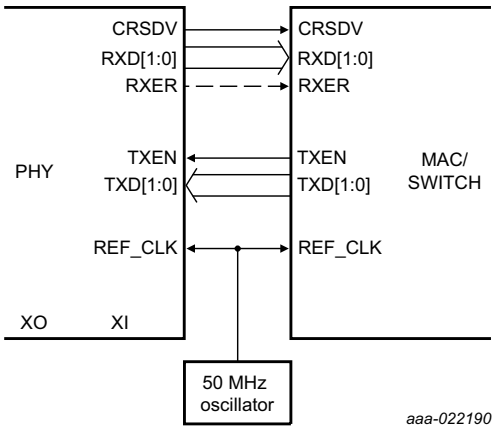
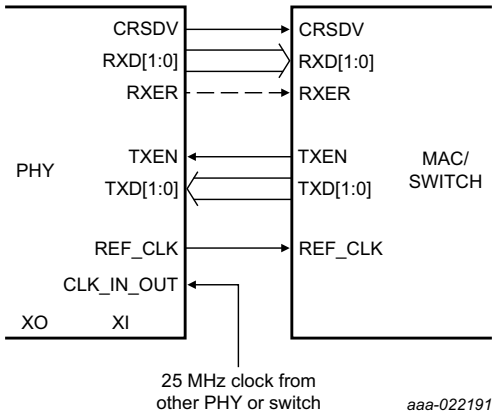


a. Using external XTAL showing optional 25 MHz clock output



b. Using external reference clock



c. Using externally generated 25 MHz reference clock

Fig 5. RMII signaling

5.2.3 Reverse MII

In Reverse MII mode, two PHYs are connected back-to-back via the MII interface to realize a repeater function on the physical layer. The MII signals are cross-connected: RX output signals from one PHY are connected to the TX inputs on the other PHY. The TXC and RXC clock signals become inputs on the PHY connected in Reverse MII mode (P0). Reverse MII mode is selected by setting bits MII_MODE = 11.

Two configuration options are available on the TJA1102. The P0 and P1 MII pins can be connected externally on the PCB (INT_REV_MII = 0). Alternatively, the MII ports can communicate via existing internal connections (INT_REV_MII = 1), as illustrated in Figure 6.

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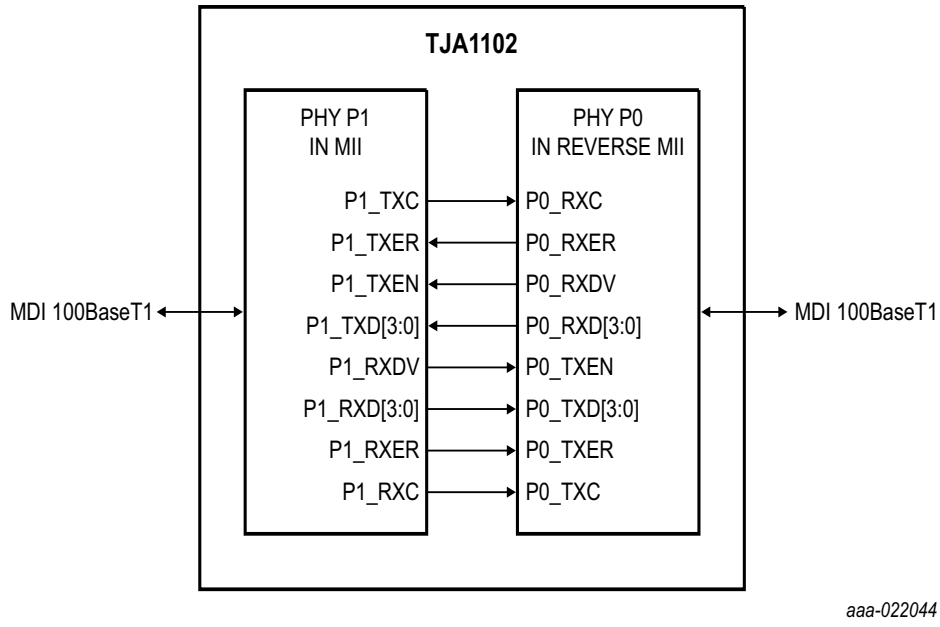

Fig 6. 100BASE-T1 repeater with TJA1102 Reverse MII

The TJA1102S can be configured in reverse MII mode by connecting the MII pins externally to a fast Ethernet product, is illustrated in Figure 7.

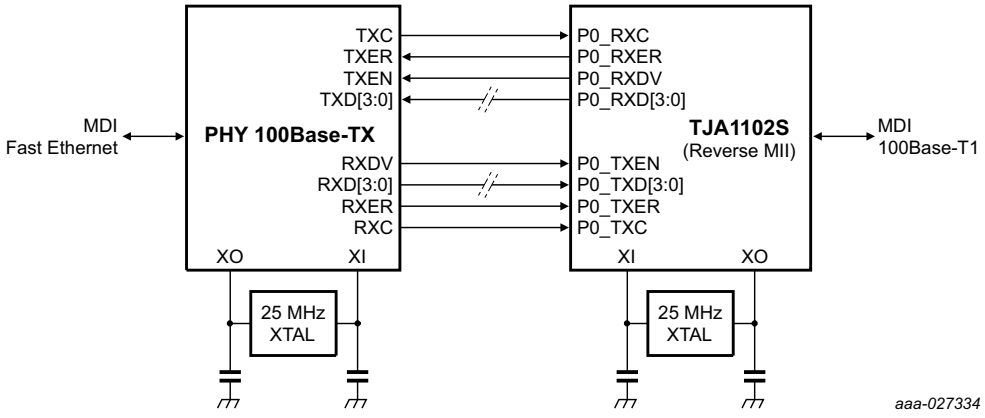

Fig 7. Fast Ethernet to 100BASE-T1 media converter with TJA1102S in Reverse MII

5.3 Sleep and wake-up forwarding concept

The sleep and wake-up forwarding concept of the TJA1102 is compliant with the OPEN Alliance Sleep wake-up specification. The TJA1102 features a wake-up request forwarding function that enables fast wake-up forwarding without the need for a switch, MAC or μC action. The wake-forwarding principle is illustrated in Figure 8. The wake-up can be forwarded via non-active (gray PHYs in the figure) or active links (white PHY). In the case of a non-active link, a wake-up pulse (WUP; duration $t_{w(wake)}$) is transmitted to be detected as activity at the link partner. For an active link, wake up request (WUR) scrambler code groups are sent.

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The wake-up behavior of the PHYs can be configured individually. This arrangement allows WAKE_IN_OUT to be used as a local wake-up or to have a mixed system with only some ports forwarding a wake-up request. The following configuration options are available and are selected via the SMI Configuration register 1:

REMWUPHY determines whether a PHY reacts to a remote wake-up request.

FWDPHYREM determines whether a PHY forwards a wake-up request (from another port or via WAKE_IN_OUT) to its MDI. A WUP or WUR is sent, depending on the link status.

LOCWUPHY determines whether a PHY should be woken up in response to a local wake-up event (forwarded from another port or via WAKE_IN_OUT)

FWDPHYLOC determines whether wake-up event should be forwarded to other ports (i.e. should the second PHY be informed and/or the WAKE_IN_OUT signal activated).

The WAKE_IN_OUT signal features a programmable timeout to enable it to support a number of wake-up concepts (e.g. wake-up line). It reacts on a rising edge.

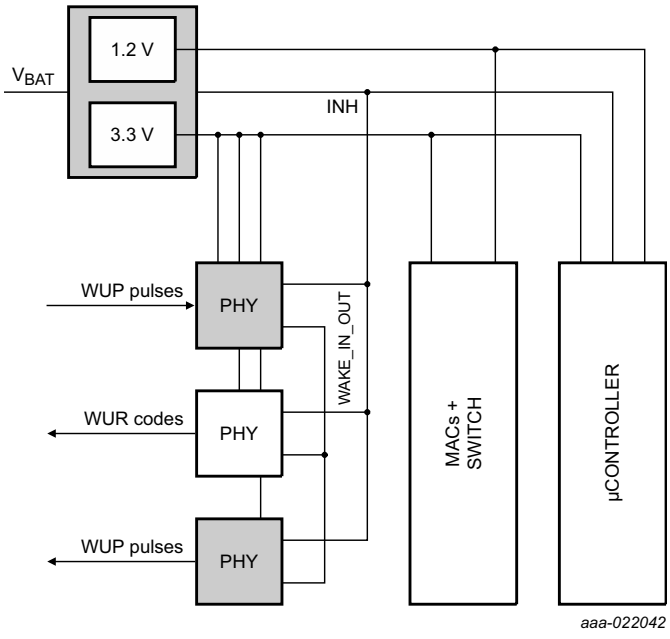

Fig 8. Wake request forwarding

6. Application information

The MDI circuit used for each PHY port is shown in Figure 9. The common mode termination depends on OEM requirements and might vary, depending on the application.

The common mode choke is expected to be compliant with the OPEN Alliance CMC specification. The 100 nF coupling capacitors should have a voltage range ≥ 50 V with 10 % (max) tolerance.

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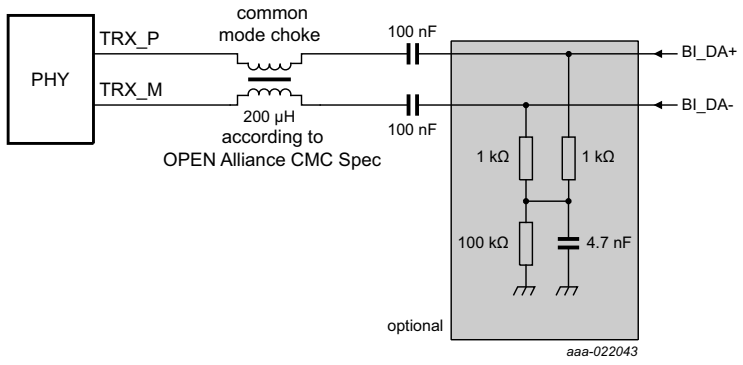

Fig 9. MDI circuit diagram

Further information can be found in the TJA1102 application hints [Ref. 2].

7. Package information

The TJA1102 comes in the HVQFN-56 package as shown in Figure 10. Measuring just 64 mm^2 with a pitch of 0.5 mm, it is particularly suited to PCB space-constrained applications, such as an integrated IP camera module. The package features wettable sides/flanks to allow for optical inspection of the soldering process. The exposed die pad shown in the package diagram should be connected to ground.

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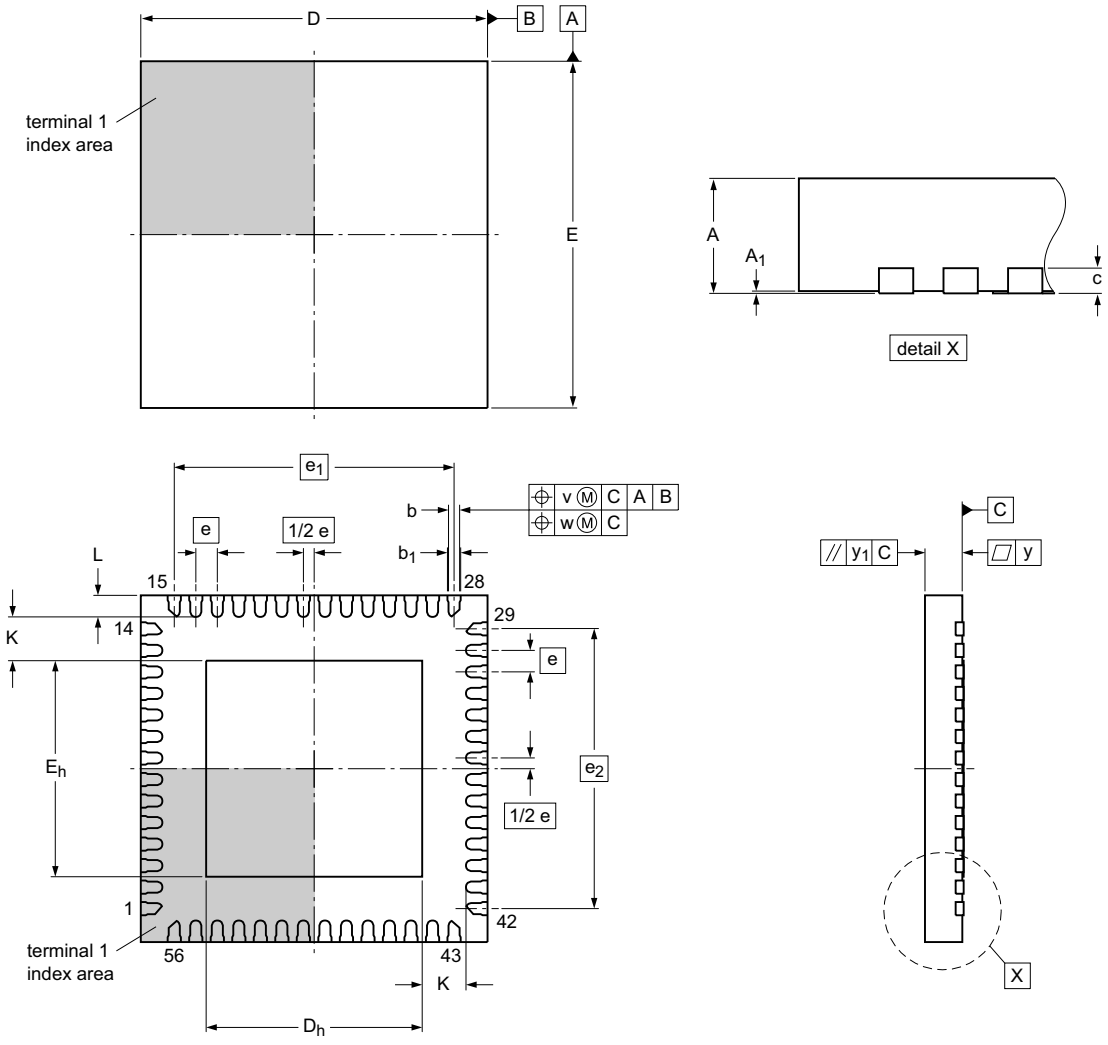
8. Package outline

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm **SOT684-13**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	b_1	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	K	v	w	y	y_1
mm	max	1.00	0.05	0.30	0.32		8.1	5.15	8.1	5.15				0.6					
	nom	0.85	0.02	0.25	0.27	0.2	8.0	5.00	8.0	5.00	0.5	6.5	6.5	0.5		0.1	0.05	0.05	0.1
	min	0.80	0.00	0.20	0.22		7.9	4.85	7.9	4.85				0.4	0.8				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot684-13_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT684-13		- - -				~~15-05-29~~ 15-07-13

Fig 10. Package outline SOT684-13 (HVQFN56)

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9. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

9.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

9.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

9.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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9.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 11) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 2 and 3

Table 2. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 3. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 11.

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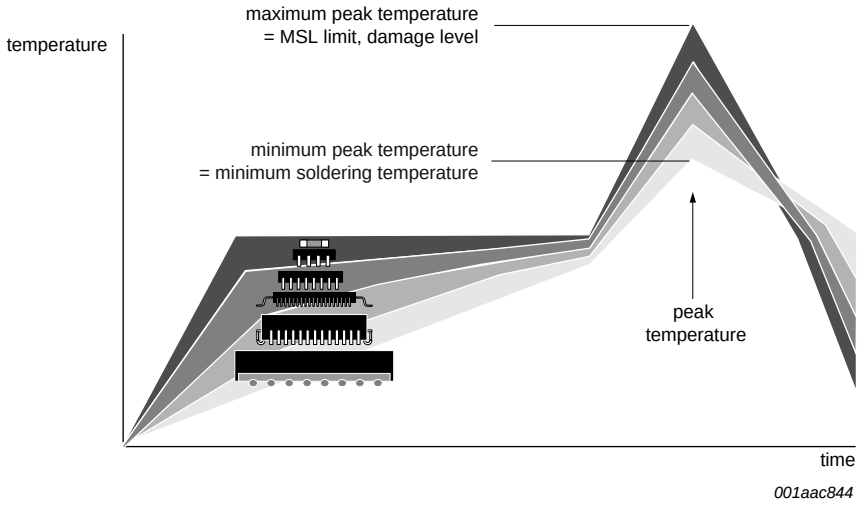

MSL: Moisture Sensitivity Level

Fig 11. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

10. References

[1] IEEE Std 802.3bw-2015, 26 October 2015

[2] AH1508_TJA1102 Application Hints

11. Revision history

Table 4. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1102_SDS v.1	20171101	Product short data sheet	-	-

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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