INTEGRATED CIRCUITS

DATA SHEET

TDA8543
2 W BTL audio amplifier

Product specification

1997 Jun 12

FEATURES

- Flexibility in use
- Few external components
- Low saturation voltage of output stage
- Gain can be fixed with external resistors
- Standby mode controlled by CMOS compatible levels
- Low standby current
- No switch-on/switch-off plops
- High supply voltage ripple rejection
- Protected against electrostatic discharge
- Outputs short-circuit safe to ground, V_{CC} and across the load
- Thermally protected.

GENERAL DESCRIPTION

The TDA8543(T) is a one channel audio power amplifier for an output power of 2 W with an 8 Ω load at a 7.5 V supply. The circuit contains a BTL amplifier with a complementary PNP-NPN output stage and standby/mute logic. The TDA8543T comes in a 16 pin SO package and the TDA8543 in a 16 pin DIP package.

APPLICATIONS

- Portable consumer products
- Personal computers
- Telephony.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		2.2	5	18	V
I_q	quiescent current	V_{CC} = 5 V	–	8	12	mA
I_{stb}	standby current		–	–	10	μA
P_o	output power	THD = 10%				
		R_L = 8 Ω; V_{CC} = 5 V	1	1.2	–	W
		R_L = 8 Ω; V_{CC} = 7.5 V	–	2.2	–	W
		R_L = 16 Ω; V_{CC} = 9 V	–	2.0	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	–	%
SVRR	supply voltage ripple rejection		50	–	–	dB

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8543T	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
TDA8543	DIP16	plastic dual in-line package; 16 leads (300 mil); long body	SOT38-1

BLOCK DIAGRAM

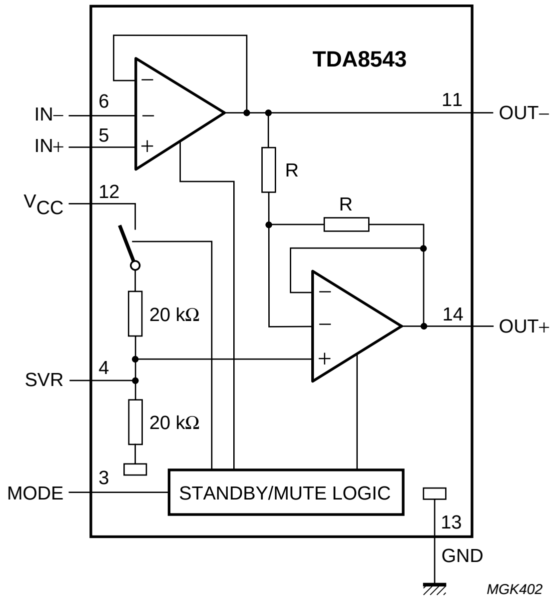


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
MODE	3	operating mode select (standby, mute, operating)
SVR	4	half supply voltage, decoupling ripple rejection
IN+	5	positive input
IN–	6	negative input
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
OUT–	11	negative loudspeaker terminal
V_{CC}	12	supply voltage
GND	13	ground
OUT+	14	positive loudspeaker terminal
n.c.	15	not connected
n.c.	16	not connected

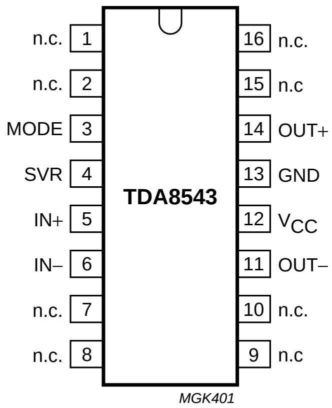


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA8543(T) is a BTL audio power amplifier capable of delivering an output power between 1 and 2 W, depending on supply voltage, load resistance and package. Using the MODE pin the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism.
The gain can be set within a range from 6 dB to 30 dB by external feedback resistors.

Power amplifier

The power amplifier is a Bridge Tied Load (BTL) amplifier with a complementary PNP-NPN output stage.

The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor, on the negative side the saturation voltage of an NPN power transistor.

Mode select pin

The device is in standby mode (with a very low current consumption) if the voltage at the MODE pin is >(V_{CC} – 0.5 V), or if this pin is floating. At a MODE voltage level of less than 0.5 V the amplifier is fully operational.
In the range between 1.5 V and V_{CC} – 1.5 V the amplifier is in mute condition. The mute condition is useful to suppress plop noise at the output, caused by charging of the input capacitor.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

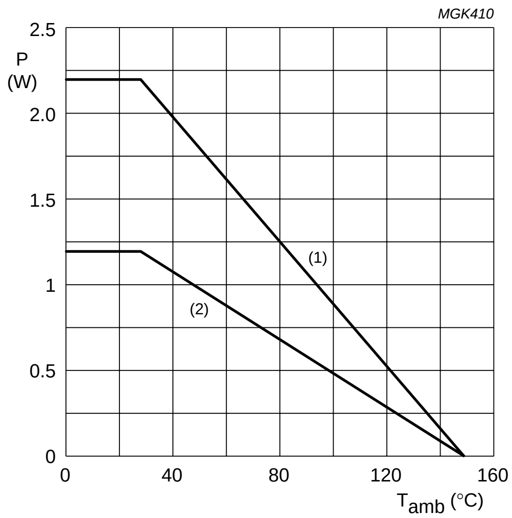
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	–0.3	+18	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		–	1	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	operating ambient temperature		–40	+85	°C
V_{psc}	AC and DC short-circuit safe voltage		–	10	V
P_{tot}	total power dissipation	SO16	–	1.2	W
		DIP16	–	2.2	W

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*. The number of the quality specification can be found in the *“Quality Reference Handbook”*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air		
	TDA8543T (SO16)		100	K/W
	TDA8543 (DIP16)		55	K/W



(1) DIP16.
(2) SO16.

Fig.3 Power derating curve.

Table 1

V_{CC} (V)	R_L (Ω)	P_o (W)(1)	CONTINUOUS SINE WAVE DRIVEN		
			P_{max} (W)	$T_{amb(max)}$ (°C)	
				SO16	DIP16
5	8	1.2	0.7	80	112
7.5	8	2.2	1.6	–	62
7.5	16	1.4	0.9	60	100
9	16	2.0	1.3	–	78
9	25	1.3	0.9	60	100

Note

1. At THD = 10%; BTL.

DC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; G = 20 dB; measured in test circuit Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	operating	2.2	5	18	V
I_q	quiescent current	$R_L = \infty$; note 1	–	8	12	mA
I_{stb}	standby current	$V_{MODE} = V_{CC}$	–	–	10	μA
V_O	DC output voltage	note 2	–	2.2	–	V
$\lvert V_{OUT+} - V_{OUT-} \rvert$	differential output voltage offset		–	–	50	mV
I_{IN+}, I_{IN-}	input bias current		–	–	500	nA
V_{MODE}	input voltage mode select	operating	0	–	0.5	V
		mute	1.5	–	$V_{CC} - 1.5$	V
		standby	$V_{CC} - 0.5$	–	V_{CC}	V
I_{MODE}	input current mode select	$0 < V_{MODE} < V_{CC}$	–	–	20	μA

Notes

1. With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.
2. The DC output voltage with respect to ground is approximately $0.5 \times V_{CC}$.

AC CHARACTERISTICS

V_{CC} = 5 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; G = 20 dB; measured in test circuit Fig.4; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
P_o	output power	THD = 10%;				
		V_{CC} = 5 V; R_L = 8 Ω	1	1.2	–	W
		V_{CC} = 7.5 V; R_L = 8 Ω	–	2.2	–	W
		V_{CC} = 9 V; R_L = 16 Ω	–	2.0	–	W
		THD = 0.5%;				
		V_{CC} = 5 V; R_L = 8 Ω	0.6	0.9	–	W
		V_{CC} = 7.5 V; R_L = 8 Ω	–	1.7	–	W
		V_{CC} = 9 V; R_L = 16 Ω	–	1.4	–	W
THD	total harmonic distortion	P_o = 0.5 W	–	0.15	0.3	%
G_v	closed loop voltage gain	note 1	6	–	30	dB
Z_i	differential input impedance		–	100	–	kΩ
V_{no}	noise output voltage	note 2	–	–	100	μV
SVRR	supply voltage ripple rejection	note 3	50	–	–	dB
		note 4	40	–	–	dB
V_o	output voltage in mute condition	note 5	–	–	200	μV

Notes to the AC characteristics

1. Gain of the amplifier is $2 \times \frac{R2}{R1}$ in test circuit of Fig.4.
2. The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance of $R_S = 0\ \Omega$ at the input.
3. Supply voltage ripple rejection is measured at the output, with a source impedance of $R_S = 0\ \Omega$ at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
4. Supply voltage ripple rejection is measured at the output, with a source impedance of $R_S = 0\ \Omega$ at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.
5. Output voltage in mute position is measured with an input voltage of 1 V (RMS) in a bandwidth of 20 kHz, so including noise.

TEST AND APPLICATION INFORMATION

Test conditions

Because the application can be either Bridge Tied Load (BTL) or Single-Ended (SE), the curves of each application are shown separately.

The thermal resistance = 55 K/W for the DIP16 envelope; the maximum sine wave power dissipation for T_{amb} = 25 °C is:

$$\frac{150 - 25}{55} = 2.27\ \text{W}$$

For T_{amb} = 60 °C the maximum total power dissipation is:

$$\frac{150 - 60}{55} = 1.63\ \text{W}$$

See the power derating curve illustrated in Fig.3.

BTL application

T_{amb} = 25 °C if not specially mentioned, V_{CC} = 5 V, f = 1 kHz, $R_L = 8\ \Omega$, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz.

The BTL application diagram is shown in Fig.4.

The quiescent current has been measured without any load impedance. The total harmonic distortion as a function of frequency was measured with a low-pass filter of 80 kHz. The value of capacitor C2 influences the behaviour of the SVRR at low frequencies, increasing the value of C2 increases the performance of the SVRR. The figure of the mode select voltage (V_{ms}) as a function of the supply voltage shows three areas; operating, mute and standby. It shows, that the DC-switching levels of the mute and standby respectively depends on the supply voltage level.

SE application

T_{amb} = 25 °C if not specially mentioned, V_{CC} = 7.5 V, f = 1 kHz, $R_L = 4\ \Omega$, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz.

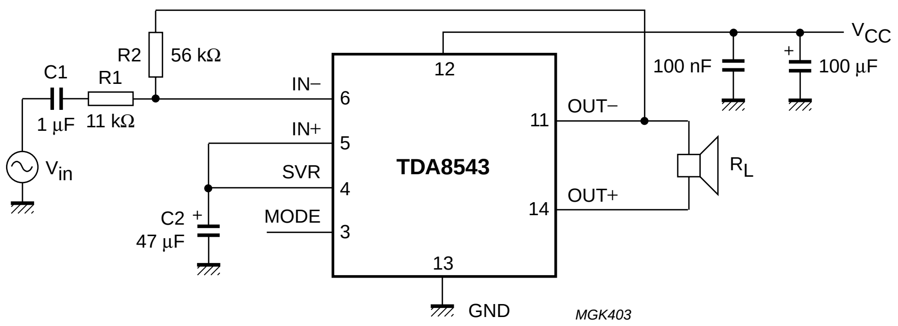
The SE application diagram is shown in Fig.14.

The capacitor value of C3 in combination with the load impedance determines the low frequency behaviour. The total harmonic distortion as a function of frequency was measured with low-pass filter of 80 kHz. The value of capacitor C2 influences the behaviour of the SVRR at low frequencies, increasing the value of C2 increases the performance of the SVRR.

General remark

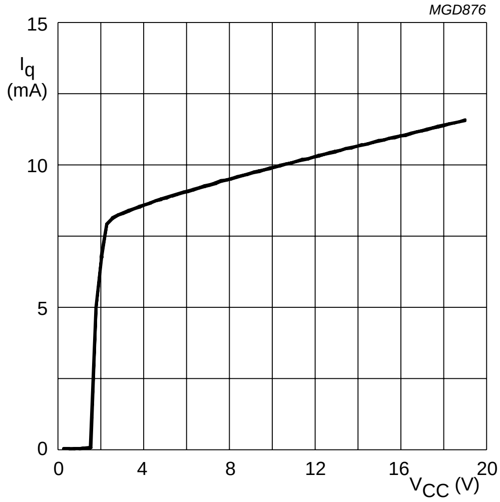
The frequency characteristic can be adapted by connecting a small capacitor across the feedback resistor. To improve the immunity of HF radiation in radio circuit applications, a small capacitor can be connected in parallel with the feedback resistor; this creates a low-pass filter.

BTL APPLICATION



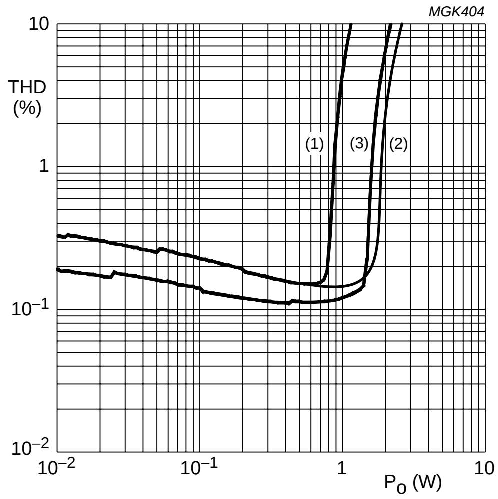
$$\text{Gain} = 2 \times \frac{R2}{R1}$$

Fig.4 BTL application.



$R_L = \infty$.

Fig.5 I_q as a function of V_{CC}.



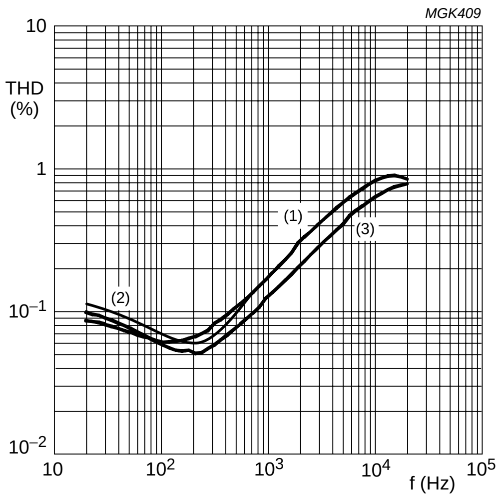
f = 1 kHz, G_v = 20 dB.

(1) V_{CC} = 5 V, R_L = 8 Ω.

(2) V_{CC} = 7.5 V, R_L = 8 Ω.

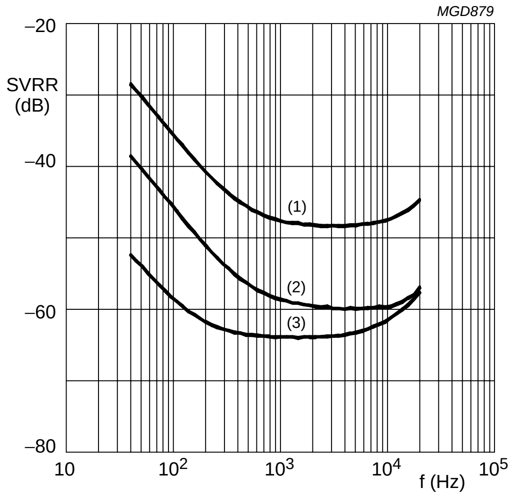
(3) V_{CC} = 9 V, R_L = 16 Ω.

Fig.6 THD as a function of P_o.



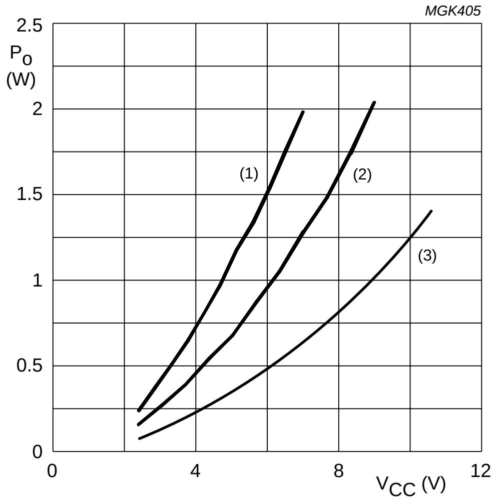
P_o = 0.5 W, G_v = 20 dB.
(1) V_{CC} = 5 V, R_L = 8 Ω.
(2) V_{CC} = 7.5 V, R_L = 8 Ω.
(3) V_{CC} = 9 V, R_L = 16 Ω.

Fig.7 THD as a function of frequency.



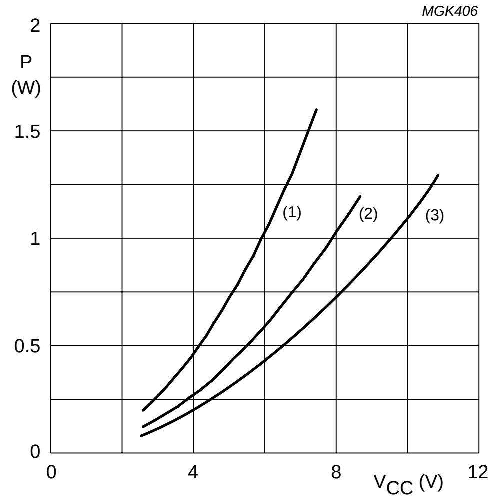
V_{CC} = 5 V, 8 Ω, R_s = 0 Ω, V_r = 100 mV.
(1) G_v = 30 dB.
(2) G_v = 20 dB.
(3) G_v = 6 dB.

Fig.8 SVRR as a function of frequency.



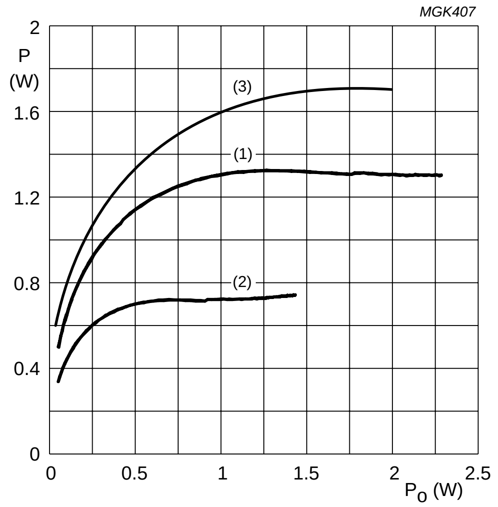
THD = 10%.
(1) R_L = 8 Ω.
(2) R_L = 16 Ω.
(3) R_L = 25 Ω.

Fig.9 P_o as a function of V_{CC}.



(1) R_L = 8 Ω.
(2) R_L = 16 Ω.
(3) R_L = 25 Ω.

Fig.10 Worst case power dissipation as a function of V_{CC}.



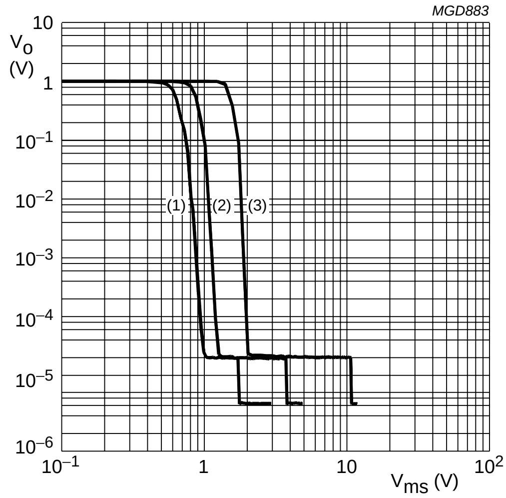
Sine wave of 1 kHz.

(1) V_{CC} = 9 V, R_L = 16 Ω.

(2) V_{CC} = 5 V, R_L = 8 Ω.

(3) V_{CC} = 7.5 V, R_L = 8 Ω.

Fig.11 P as a function of P_o.



Band-pass = 22 Hz to 22 kHz.

(1) V_{CC} = 3 V.

(2) V_{CC} = 5 V.

(3) V_{CC} = 12 V.

Fig.12 V_o as a function of V_{ms}.

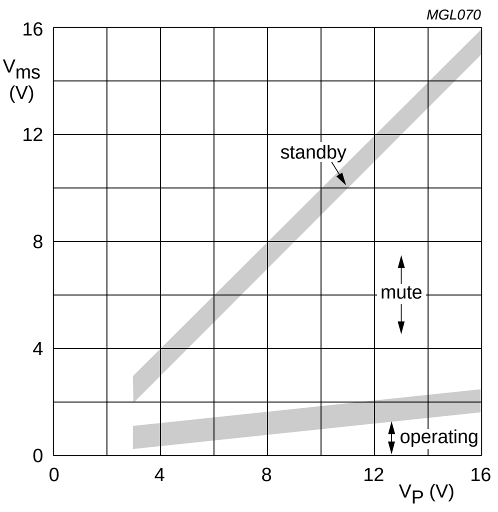
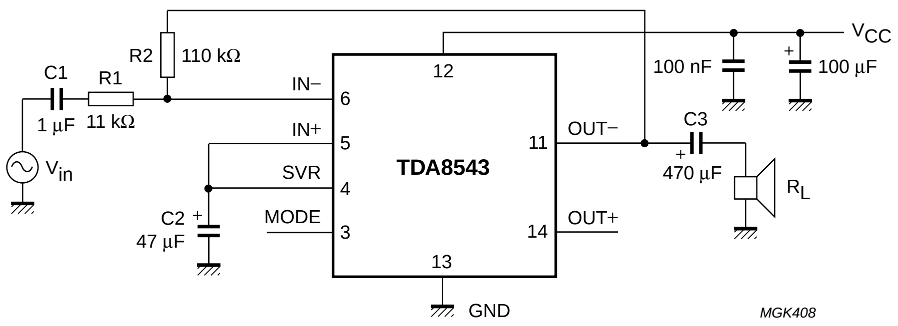


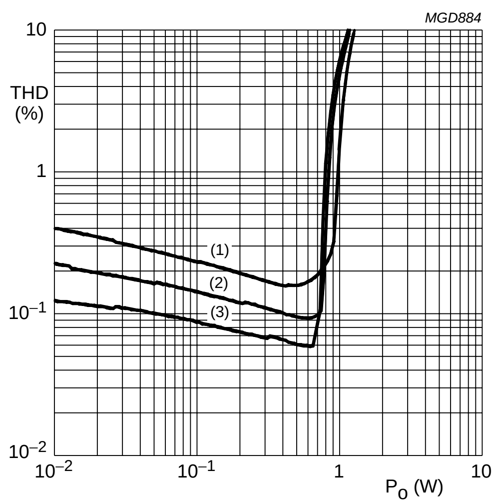
Fig.13 V_{ms} as a function of V_P.

SE APPLICATION



Gain = $\frac{R2}{R1}$

Fig.14 SE application.



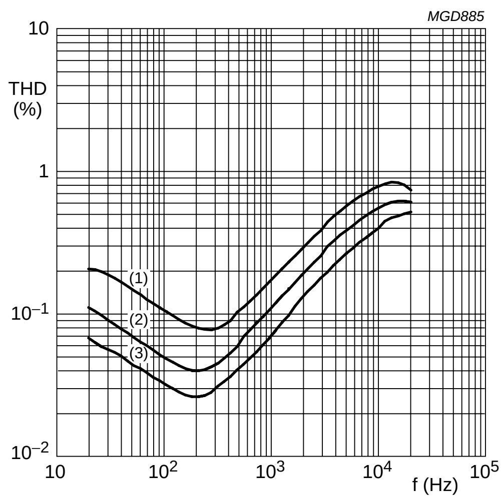
f = 1 kHz, G_v = 20 dB.

(1) V_{CC} = 7.5 V, R_L = 4 Ω.

(2) V_{CC} = 9 V, R_L = 8 Ω.

(3) V_{CC} = 12 V, R_L = 16 Ω.

Fig.15 THD as a function of P_o.



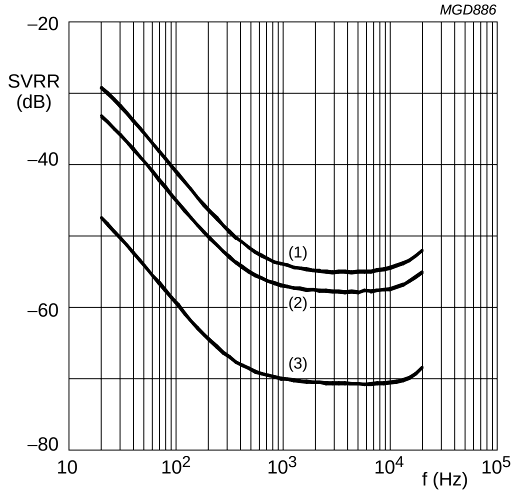
P_o = 0.5 W, G_v = 20 dB.

(1) V_{CC} = 7.5 V, R_L = 4 Ω.

(2) V_{CC} = 9 V, R_L = 8 Ω.

(3) V_{CC} = 12 V, R_L = 16 Ω.

Fig.16 THD as a function of frequency.



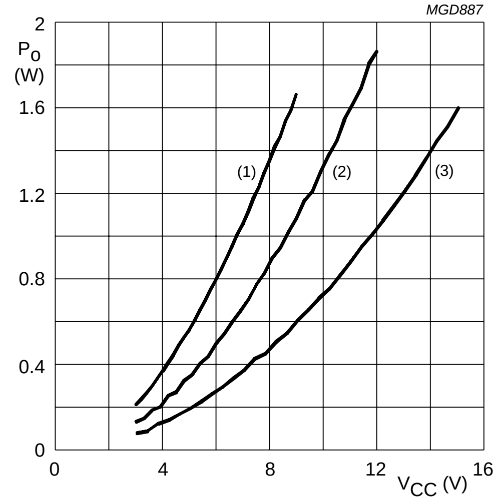
V_{CC} = 7.5 V, R_L = 4 Ω, R_s = 0 Ω, V_i = 100mV.

(1) G_v = 24 dB.

(2) G_v = 20 dB.

(3) G_v = 0 dB.

Fig.17 SVRR as a function of frequency.

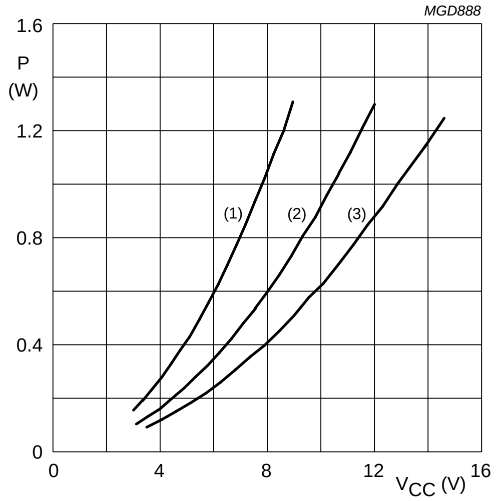


(1) THD = 10%, R_L = 4 Ω.

(2) THD = 10%, R_L = 8 Ω.

(3) THD = 10%, R_L = 16 Ω.

Fig.18 P_o as a function of V_{CC}.

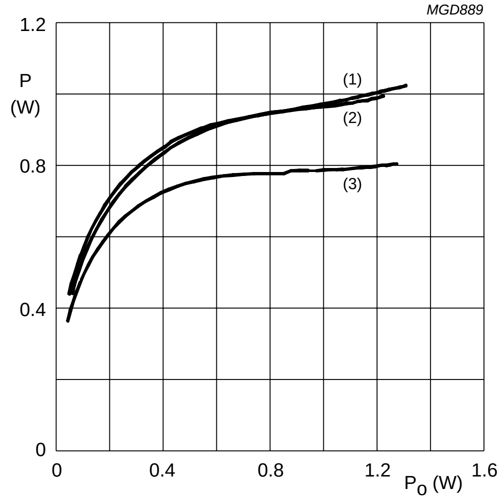


(1) R_L = 4 Ω.

(2) R_L = 8 Ω.

(3) R_L = 16 Ω.

Fig.19 Worst case power dissipation as a function of V_{CC}.

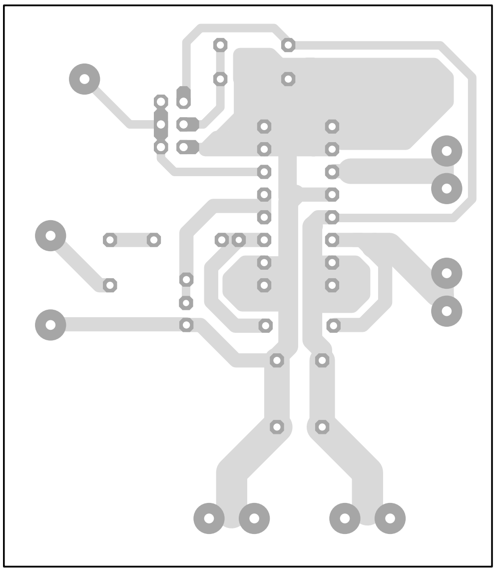


(1) V_{CC} = 7.5 V, R_L = 4 Ω.

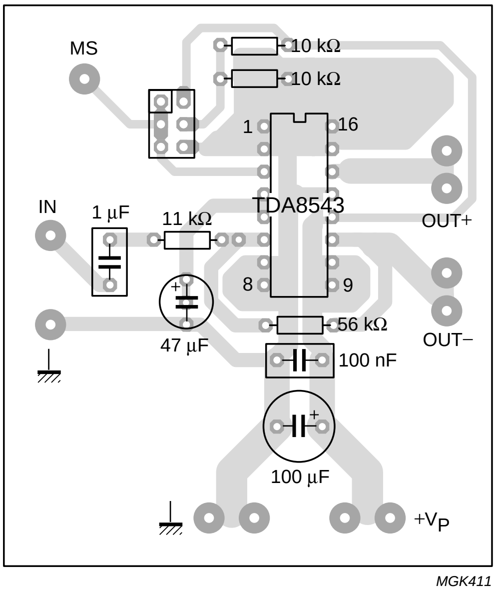
(2) V_{CC} = 12 V, R_L = 16 Ω.

(3) V_{CC} = 9 V, R_L = 8 Ω.

Fig.20 P as a function of P_o.



a. Top view.

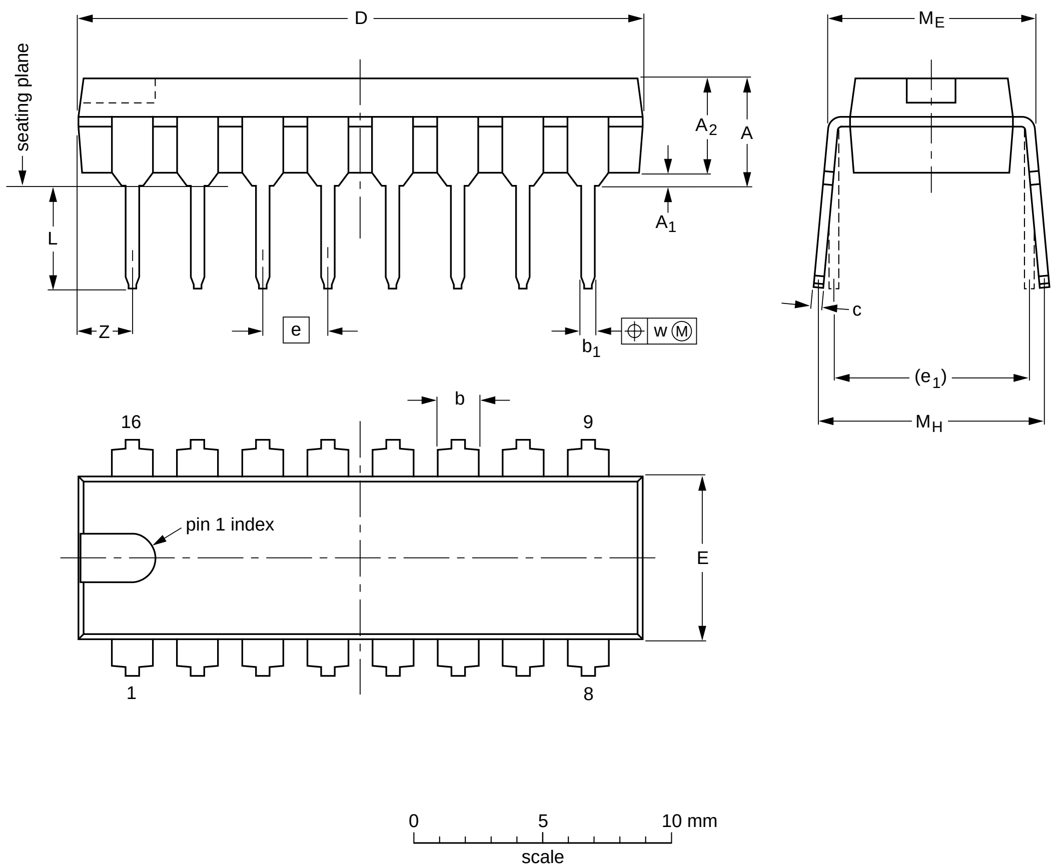


b. Component side.

Fig.21 Printed-circuit board layout (BTL and SE).

PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil); long body — SOT38-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

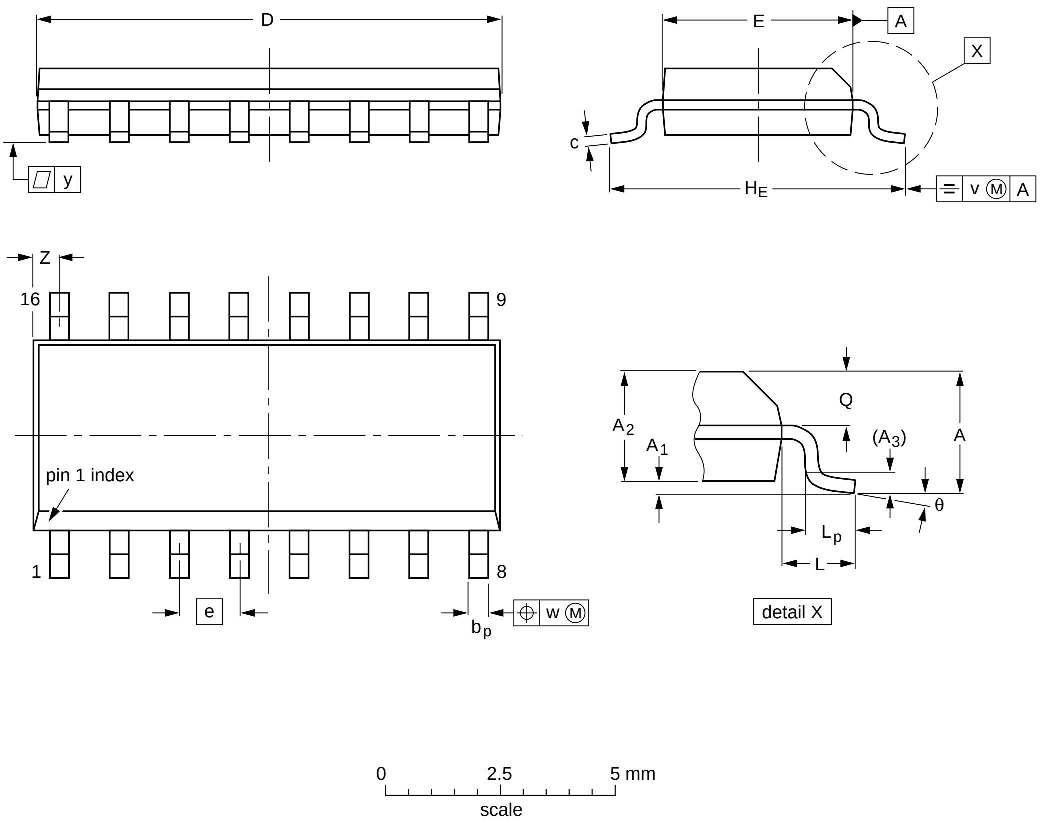
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.02	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.1	0.3	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-1	050G09	MO-001	SC-503-16			~~99-12-27~~ 03-02-13

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DATA SHEET STATUS

DOCUMENT STATUS(1)	PRODUCT STATUS(2)	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

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